Science and technology of ferroelectric films and heterostructures for non-volatile ferroelectric memories

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Abstract

We present in this article a review of the status of thin film ferroelectric materials for nonvolatile memories. Key materials issues relevant to the integration of these materials on Si wafers are discussed. The effect of film microstructure and electrode defect chemistry on the ferroelectric properties relevant to a high density nonvolatile memory technology are discussed. The second part of this review focuses on approaches to integrate these capacitor structures on a filled poly-Si plug which is a critical requirement for a high density memory technology. Finally, the use of novel surface probes to study and understand broadband polarization dynamics in ferroelectric thin films is also presented. © 2001 Published by Elsevier Science B.V.

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1. Introduction

At the dawn of a new millennium, we are witnessing the coming age of one of the major fields of research of the past century, i.e. the field of ferroelectrics. Major advances were made in the last decade in research related to the synthesis, characterization, and determination of processing-microstructure-property relationships of ferroelectric thin films and their integration into functional heterostructures. The high dielectric permittivities of perovskite-type materials can be used in dynamic random access memories (DRAM) [1–6], while the large values of switchable remnant polarization of ferroelectric materials are suitable for non-volatile ferroelectric random access memories (NVFRAM) [2–15]. The research performed during the last decade has focused on developing both the scientific bases for the synthesis and characterization of ferroelectric capacitor heterostructures and the applications to ferroelectric film-based memories [1–15].

The technological uses of oxide thin films are not limited to ferroelectric memories, but extend to a wide range of applications in discrete devices, utilizing the full range of properties, including dielectric, ferroelectric, piezoelectric, electrostrictive, pyroelectric, optical, electro-optic and magnetic properties, as well as electronic conduction, ionic conduction and superconductivity. Applications include multilayer capacitors for memories, piezoelectric film-based microelectro-mechanical systems (MEMS), boundary layer capacitors, varistors, gas sensors, radiation detectors,
temperature sensors, transducers, switches, shutters, MHD electrodes, fuel cell electrolytes, concentration cell electrolytes and electrolytes for high energy density batteries. These ceramics represent an important world market, which has been experiencing steady growth [16].

The major scientific and technological advances produced in the last 11 years in materials science and devices related to the field of ferroelectric thin films have been possible because of substantial advances in the development and optimization of thin film deposition techniques, as well as the development of novel materials integration strategies and device concepts. As indicated above, ferroelectric thin films play a major role in a large variety of devices. However, NVFRM represent the first ferroelectric thin film-based device introduced into a mass consumption market in the form of low density-memory ‘smart cards’ [17]. Therefore, this article is dedicated to reviewing major advances made in the science and technology related to NVFRAM.

Over the past decade, many significant advances in thin film deposition techniques have occurred. Various physical vapor phase deposition techniques (plasma and ion beam sputter-deposition (PSD and IBSD), pulsed laser ablation deposition (PLAD), electron beam or oven-induced evaporation for molecular beam epitaxy (MBE), metalorganic chemical vapor deposition (MOCVD)), and chemical solution methods (e.g. sol–gel processing and metalorganic deposition (MOD)) have been optimized and extensively used in the past 11 years to investigate the synthesis of ferroelectric films and layered heterostructures [5–17]. However, MOD is currently used for the deposition of ferroelectric thin films for fabrication of low density NVFRAM, while MOCVD is the forerunner for ferroelectric films in high density NVFRAM. In spite of the progress in the development and application of the various film deposition techniques mentioned above, work is still necessary to optimize the deposition parameters and conditions for most of them. A major issue in relation to film synthesis by any of the methods described above is the difficulty in reliably producing device-quality films directly on large semiconductor substrates, in a way that is fully compatible with existing semiconductor process technology. Issues related to deposition techniques are reviewed in this article in view of work performed in several laboratories worldwide.

Film synthesis techniques discussed in this review include sputter-deposition, laser ablation-deposition and MOCVD, since they represent three of the most utilized deposition methods in relation to the science and technology of ferroelectric thin films. All three techniques can produce films with device-quality characteristics. A manufacturing process for producing ferroelectric thin film-based devices should at least include the following characteristics: (1) applicability of the processes to deposition of ferroelectric films and integration with metallic or conductive oxide electrode layers with different physical and chemical properties; (2) compatibility with integrated device processing, including production of as-deposited films with specific microstructures (perovskite, for example) on substrates at the lowest possible temperature; (3) production of device-compatible, highly oriented or polycrystalline films and heterostructures with specific properties (e.g. fatigue-free for a large number of polarization switching cycles, long polarization retention times, and no polarization imprint effects); (4) ability to produce patterned structures, superlattices and layered heterostructures; (5) reproducibility of the deposition process and (6) simple and low cost deposition processes with capacity for high deposition rates.

Another major subfield of research related to the science and technology of ferroelectric thin films and heterostructures is that involving the development of materials integration approaches to produce capacitors with memory-compatible properties and their integration with semiconductor devices to fabricate NVFRAM. Therefore, another focus of this review is on materials integration approaches for the production of ferroelectric capacitors and their incorporation into semiconductor wafers for the fabrication of NVFRAM.
Finally, major advances in memory concepts and implementation are critically reviewed and considered in view of future developments. Many university, national and industrial laboratories have made major contributions to the science and technology of ferroelectric thin films and devices. However, due to the rapid pace of R&D in this field, it is almost impossible to describe all the work performed by groups around the world. Therefore, we apologize if some references have been overlooked.

2. Ferroelectric thin film deposition and characterization

2.1. Magnetron sputter-deposition and characterization of ferroelectric thin films and heterostructures

Several variations of the PSD technique have been developed and are still being optimized for the production of multicomponent oxide thin films, including HTSC ferroelectric, and electro-optic materials. The PSD techniques described in this review are being developed both for use in research laboratories and for commercial production of thin film-based devices. Basic phenomena occurring during the interaction of plasmas with the targets and substrates, during film synthesis, are important in that they determine to a large extent the composition, microstructure, and properties of the films.

Extensive work has been performed in recent years on PSD of ferroelectric thin films. Both single multicomponent oxide and multiple elemental metallic target have been used to synthesize a wide range of ferroelectric materials in thin film form, including BaTiO₃ (BTO) [18], Ba₅Sr₁−ₓTiO₃ (BST) [19,20], PbTiO₃ (PT) [21], PbₓLaₓTiO₃ (PLT) [22], Pb(ZrₓTi₁−ₓ)O₃ (PZT) [23] and PbₓLaₓ(ZrₓTi₁−ₓ)O₃ (PLZT) [24] and SrBi₂Ta₂O₉ (SBT) [25]. Early work demonstrated that highly c-axis oriented PT thin films can be produced by rf magnetron sputtering only when using low deposition rates (<20 Å min⁻¹), gas pressure of about 7 × 10⁻³ Torr and PbO-rich targets [22]. These results were explained on the basis that high gas pressures in the magnetron system increase the sputtering rate because of the production of a larger amount of ions in the plasma, while simultaneously decreasing the mean kinetic energy of the sputtered species arriving at the substrate, due to collisions with the plasma species. A reduced kinetic energy of the depositing species results in a lower mobility on the substrate surface at the deposition temperature. The combination of high sputtering rate (hence high deposition rate) and low mobility of the depositing species tend to inhibit the epitaxial growth of the film. This work [22] demonstrated the importance of controlling the deposition parameters to optimize film properties for particular device applications.

Magnetron sputtering was also used to produce PZT films with controlled stoichiometry and properties, utilizing metallic elemental targets [24]. The growth of stoichiometric, highly oriented films via the elemental target magnetron sputter-deposition method is governed by three main processes: (1) formation of a reproducible oxide layer on the target surface; (2) the stability of oxide species formed during transport through the plasma towards the substrate and (3) the nucleation and growth of the film on the substrate surface. Computer simulations of the transport of sputtered species in the plasma and experimental measurements of deposition rate versus gas pressure and film composition versus substrate-target distance indicated that complex plasma–surface interaction and material transport processes control many of the film characteristics, including film composition, microstructure and resulting electrical properties [24].

Magnetron sputter-deposition has also been used to synthesize layered perovskite films. The material most extensively investigated has been SBT [8], since SBT-based capacitors, using Pt electrodes, exhibit practically no fatigue, long polarization retention, low leakage, and negligible
imprint, all necessary properties for capacitors to be integrated with semiconductor devices to fabricate the first generation of NVFRAM. SBT films have been synthesized by magnetron sputter-deposition on Pt/Ti/Si substrates. The Pt/Ti electrode technology has been extensively used by many groups [5–13]. A general observation related to the synthesis of SBT films on Pt/Ti electrode layers, using magnetron sputter-deposition, has been that these films need to be deposited at \(<400^\circ\text{C}\) and subsequently annealed to about 750–800\(^{\circ}\text{C}\) to produce the layered perovskite structure [25]. However, recent work [7–22] demonstrated that the Pt/Ti electrode technology is not appropriate for reliable NVFRAM capacitors. Recent experimental work involving studies of film growth processes via IBSD in conjunction with in situ time-of-flight ion scattering and direct recoil spectroscopy has provided insight into this issue (see Section 2.2). However, SBT-based capacitors with appropriate microstructure and good electrical properties have been produced, using the magnetron sputter-deposition method [25] (see Fig. 1).

![Graph](image_url)

**Fig. 1.** Data showing the orientation of an SBT layer (XRD spectrum) (a) and polarization hysteresis curves for various voltages (b) of a Pt/SBT/Pt capacitor produced using a magnetron sputter-deposition technique [25].
The limited discussion of plasma sputter-synthesis of ferroelectric thin films presented above indicates that the geometry and deposition conditions play fundamental roles in the synthesis of ferroelectric thin films by PSD. Unfortunately, there is not enough systematic data related to the sputter-synthesis technique, particularly related to the sputtering, species transport, and deposition processes, for many of the ferroelectric materials being investigated, to synthesize films under well-controlled conditions. Therefore, further work is necessary to understand these processes and determine the optimum conditions needed to produce films of different ferroelectric materials with the best composition, microstructure, and properties, using PSD methods. This work would be relevant from the basic science point of view, since it is now widely accepted that MOCVD is the film synthesis technique to be used in NVFRAM manufacturing.

2.2. Ion beam sputter-deposition and characterization of ferroelectric thin films and heterostructures

IBSD has been used as a versatile method for investigating the synthesis of ferroelectric thin films and heterostructures. Multiple ion beam-multi-target [26] and single ion beam, multi-target (SIBMT) [27] deposition techniques were developed and extensively used to synthesize ferroelectric and metallic thin films and heterostructures. Specifically, the SIBMT method was used to produce heterostructure capacitors with metal, conductive oxide, and hybrid metal-oxide electrodes [28,29] in studies focused on controlling polarization fatigue, retention and imprint. The IBSD technique, in any of the variations described above, has several advantages over PSD methods, namely: (1) independent control of ion current density and energy, which can be used to control the sputtering process and consequent film characteristics; (2) lower operating pressure in the deposition chamber and minimization of the plasma-substrate interaction, which can produce undesirable effects, such as resputtering of the film, damage, and gas incorporation during film deposition; (3) ability to control the composition of the films by tailoring the deposition of each elemental material; (4) ability to produce smoother films because of better control of the deposition rate. However, the IBSD technique is not being used as a standard fabrication method in the microelectronic industry (primarily due to lower deposition rates), while the magnetron sputtering method is extensively used, particularly for metallization of microcircuits.

2.2.1. Processing–microstructure–property relationships of ferroelectric PZT thin films and heterostructures

It became clear in the last 4 years that the two most promising ferroelectric materials for application to the first generation of NVFRAM are PZT and SBT. Both materials have been used to fabricate capacitors with practically no polarization fatigue, long polarization retention, negligible imprint, and low leakage. Fatigue-free SBT-based capacitors have been produced using Pt electrodes. On the other hand, PZT-based capacitors exhibit large polarization fatigue, after about $10^6$–$10^7$ switching cycles, and substantial polarization retention loss when used in conjunction with Pt electrodes. However, the integration of metal-oxide electrodes (e.g. RuO$_2$, hybrid Pt/RuO$_2$ [28,29], SrRuO$_3$ [30,31], La$_{0.5}$Sr$_{0.5}$CoO$_3$ (LSCO), hybrid Pt/LSCO [32,33] and Y–Ba–Cu–O [34] with PZT films into heterostructure capacitors provided the means to control fatigue and retention in PZT-based capacitors. The work recently performed by various groups indicates that electrode material and orientation, and/or the Pt electrode interface (including intermediate template layers) [28–34] are key factors involved in the control of orientation of the ferroelectric layer and electrical properties of PZT-based heterostructure capacitors. Electrical characterization of PZT-based capacitors synthesized using a PbTiO$_3$ (PT) template layer at the bottom or top electrode/PZT
interfaces revealed substantial differences in their fatigue behavior. Capacitors without the PT layer exhibit a substantial fatigue (about 71% reduction in remnant polarization), while those with one or two PT layers have a substantially smaller fatigue (about 34 and 29% decrease, in remnant polarization, for one and two PT layers, respectively, Fig. 2(a)) [28,29]. The incorporation of hybrid Pt/RuO$_2$ bottom electrode in the PZT capacitor, prior to producing the PT layer, results in a highly oriented (0 0 1) PZT film and negligible fatigue (≤7% reduction in remnant polarization [28,29]). In addition, Al-Shareef et al. demonstrated [29] that there is an optimum combination of individual layer thickness for RuO$_2$/Pt hybrid electrodes that yield PZT capacitors with negligible fatigue.
(Fig. 2(b)) and low leakage (Fig. 2(c)). These results indicate that template layers such as PT contribute to eliminate the formation of undesirable second non-ferroelectric phases and/or charged defects (e.g. oxygen vacancies), which can produce internal bias fields in the PZT layer or at the PZT/electrode interface, all of which may play a role in the fatigue process. The beneficial effects of the layer(s) are enhanced by the hybrid metal-RuO$_2$ bottom electrode. In any case, it is relevant to point out that in spite of the use of optimized hybrid metal-RuO$_2$ and PT layers, fatigue is not totally eliminated in the IBSD–PZT capacitors, since there is still a small decrease (~7\%) in remnant polarization after ~$10^{10}$ switching cycles. This suggests that not only the electrode material, but also the structure of the PZT/electrode interface may play a role in the fatigue process. An issue not yet addressed is whether IBSD may result in damage at the electrode/ferroelectric layers interface, due to scattered ions from the target, an effect extensively studied by one of the authors and colleagues [35]. This hypothesis is based on the fact that similar PZT-based capacitors produced by other methods, such as pulsed laser ablation-deposition and MOCVD, where ion-induced effects are absent, show practically no fatigue. Further studies of this interface, preferably at the atomic scale level using in situ characterization techniques may contribute to clarify this point.

In addition to controlling polarization fatigue, retention, and imprint phenomena in PZT-based capacitors, control of dc leakage current is very important. Measurements of dc leakage currents for PZT capacitors with various combinations of RuO$_2$, hybrid Pt/RuO$_2$, and codeposited Pt/RuO$_2$ electrodes (Fig. 2(c)) revealed that the bottom electrode layer plays a critical role in controlling leakage currents, since it controls the ferroelectric layer composition and microstructure.

2.2.2. Processing–microstructure–property relationships of ferroelectric SBT thin films and heterostructures

The IBSD method has been used also to investigate the synthesis of SBT films on various substrates, particularly in relation to understanding the initial stages of SBT growth by physical vapor-deposition. For example, Im et al. studied the initial growth of SBT films on various electrode structures such as Pt/Ti/SiO$_2$/Si, Pt/TiO$_2$/SiO$_2$/Si, Pt/Ta/SiO$_2$/Si, Ir/SiO$_2$/Si, and RuO$_2$/SiO$_2$/Si [36]. These experiments were carried out at 700°C under $p_{O_2} = 5 \times 10^{-4}$ Torr, since these are suitable parameters to synthesize SBT films via IBSD. These studies were performed using a unique time of-flight mass spectroscopy of recoil ions (MSRI) technique suitable for performing in situ characterization of film growth processes in high-pressure environments.

Fig. 3 shows the following outstanding features: (a) when SBT is deposited on a Pt/TiO$_2$/SiO$_2$/Si heterostructure bottom electrode, where no Ti nor Si segregation to the surface is observed (see absence of Ti or Si peaks in the spectrum), all three elements of Bi, Sr, and Ta are readily incorporated in the initial growth stages of a film deposited at 700°C (Fig. 3(a)); (b) when SBT is deposited on Pt/Ti/SiO$_2$/Si at 700°C, Bi is not efficiently incorporated into the SBT film, while Sr and Ta are readily incorporated (Fig. 3(b) and (c)). A comparison of the relative intensity of the Bi peaks in all three cases reveals that the Bi concentration in the 12 Å SBT film grown on Pt/TiO$_2$ is more than twice the Bi concentration on Pt/Ti with only Ti segregation (Fig. 3(b)), and more than three times the Bi concentration on Pt/Ti with Ti and Si segregation (Fig. 3(c)). Since the peak heights of the Sr and Ta are relatively similar in all three cases, it is concluded that the initial SBT films grown on PT/Ti electrodes are Bi deficient compared to the films grown on Pt/TiO$_2$ electrodes.

The inhibition of Bi incorporation on Pt surfaces with segregated Ti and Si species is due to the lower free energy of oxide formation for Ti and Si compared to Bi. That is, Ti and Si can thermodynamically reduce bismuth oxide to Bi at 700°C in an oxygen environment when mixed on the surface. Because of the high vapor pressure of Bi at high temperatures, the reduced Bi will readily evaporate from the surface. The in situ characterization of SBT film growth processes
discussed above demonstrated that Pt/Ti is an unstable bottom electrode, while Pt/TiO₂ provide a stable electrode for vapor-deposition of SBT films. In addition, these studies have proven the value of understanding vapor-phase film growth processes to control film composition, microstructure and properties.

2.3. Pulsed laser ablation-deposition and characterization of ferroelectric films and heterostructures

2.3.1. Processing–microstructure–property relationships of PZT films and integration with semiconductor substrates

The pulsed laser-ablation deposition (PLAD) technique gives researchers the capability to investigate the synthesis of multicomponent oxide thin films, including ferroelectric and associated conductive oxide layers, with controlled composition, microstructure and properties in a rapid materials prototyping manner. Extensive work has been performed to understand the physics of the PLAD method [37]. Understanding the deposition process for PZT ferroelectric film growth is important in order to minimize Pb loss during film growth, eliminate formation of pyrochlore (non-ferroelectric) phases, eliminate surface particulates, and control the film microstructure. Each of
these factors will affect device properties to some extent. Knowledge and control of the ablated flux distribution is also important for scale-up to produce uniform films on large-area substrates. Studies of the PLAD process have demonstrated that background gas pressure during deposition, substrate to target distance, laser energy and wavelength, and target-substrate relative geometric arrangement, among other parameters have a significant effect on oxide film composition, microstructure and properties. A systematic investigation of the ablation characteristics of PZT, La$_{0.5}$Sr$_{0.5}$CoO$_3$ (LSCO), and other targets relevant to the synthesis of ferroelectric capacitors were performed by various groups to understand and control film deposition parameters that play fundamental roles in controlling the composition, microstructure and properties of PZT-based capacitors for non-volatile memories. PZT was studied because of its potential as a ferroelectric material for memory device applications. LSCO was investigated, because, it is a conductive oxide material and was demonstrated to be an excellent electrode material for ferroelectric capacitors [32,33].

The power of the PLAD method for the development of materials integration strategies was demonstrated by the growth of highly oriented PLZT films on SiO$_2$/Si substrates using a Bi$_4$Ti$_3$O$_{12}$ (BTO) template layer [34]. The presence of the thermal oxide on Si is important, since it form the basis for fabricating the pass-gate transistors in the Si-CMOS wafer. Contrary to what is expected from growing a film on an amorphous surface such as SiO$_2$, the BTO layer grows completely c-axis oriented, although the film has very little crystallographic long-range correlation in the plane. The BTO layer provides a template with a perovskite structure to control the subsequent growth of the LSCO/PLZT/LSCO stack promoting the growth of the PLZT layer with [0 0 1] orientation, as illustrated in the X-ray diffraction (XRD) pattern in Fig. 4. Rocking measurements about the [0 0 2] PLZT peak show a width of about 1.0–1.2°. The efficacy of the BTO template layer to control the orientation of the over-layer is further demonstrated by the fact that even metals, such as Pt (fcc; $a = 3.92$ Å) can be grown on a BTO template with a preferred [0 0 1] orientation when deposited at the appropriate substrate temperature (400–500°C) (Fig. 4).

The main reason for the considerable interest in growing PZT-based heterostructure capacitors with oxide or hybrid metal–metallic oxide electrodes is the recent demonstration of very desirable ferroelectric properties using such structures. Many of the details of the ferroelectric properties of LSCO/PLZT/LSCO capacitors produced by the PLAD method can be found in the recently

![Fig. 4. XRD pattern of a LSCO/PLZT/LSCO/Pt/BTO heterostructure, grown on a SiO$_2$/Si substrate at 600°C. The figure shows a preferred [0 0 1] orientation of the whole heterostructure induced by the BTO template layer. The inset shows a similar X-ray scan from a PLZT/Pt heterostructure without the BTO template layer.](image)
published literature [32–34,37]. Fig. 5(a) shows pulsed hysteresis loops for a LSCO/PLZT/LSCO heterostructure grown on SiO₂/Si with the BTO template and a Pt under-layer. Typically, pulsed remnant polarization values in the range of 15–20 μC cm⁻² were obtained at room temperature, with an applied voltage of 5 V. The coercive field of the PZT-based capacitors with oxide electrodes, which is also an important memory element design variable, is typically in the range of 0.7–1.5 V. The film resistivity at 5 V is typically in the range of 5 × 10¹⁰ to 5 × 10¹¹ Ω cm, a value which is considerably higher compared to those obtained in the early days of the use of the metal oxide electrodes. This result can be attributed to better control over the deposition parameters, including the film thickness, lead deficiency, etc. The integration of LSCO or hybrid Pt-LSCO electrodes with PZT films provided a better solution to the polarization fatigue problem that plagued Pt/PZT/Pt capacitors. This is illustrated in Fig. 5(b), for the case of a LSCO/PLZT/LSCO/Pt capacitor grown on a SiO₂/Si substrate, where fatigue-free conditions are observed after 10¹² polarization switching cycles. The marked difference in fatigue characteristics with the type of electrode (i.e. Pt or metal oxide) is observed irrespective of the crystalline quality of the PLZT thin film.

Another important parameter related to the reliable electrical behavior of a capacitor for non-volatile memories is the polarization retention as a function of time after a capacitor has been polarized in one logic state. Retention tests are typically performed using a sequence of pulses (for example, −5 V write; 4 V read; 4 V read) with temperature as one critical external variable. Under these test conditions, the first read pulse probes a switched polarization (P⁺), i.e. the logic state ‘1’, indicating the ability to maintain a polarization charge in the logic state ‘1’. The second read pulse probes the non-switched polarization (P⁻), which corresponds to the logic state ‘0’. The switched
polarization ($\Delta P = P^* - P^\wedge$) followed a log-linear relationship with retention time. The capacitors tested under the conditions described above presented sufficient difference in the polarization values ($\Delta P$, 10–12 $\mu$C cm$^{-2}$) between the logic state ‘1’ and ‘0’ after five decades of waiting time, which, when extrapolated, accounts for several years of device operation. Data retention (which is ferroelectric capacitors manifests itself as a relaxation of the remnant polarization state) is probably the most important property that is desired for the ferroelectric film and the capacitor. However, fundamental understanding of this relaxation process has not revived as much attention as the phenomena of fatigue and imprint (which is described below). Indeed, there is very little microscopic understanding of how the relaxation occurs. Some insights on this process are described in Section 4.

Another major NVFRAM operation-related parameter that needs to be controlled is imprint. Imprint is a tendency of the ferroelectric capacitor (or the memory element) to revert to one preferred state. For example, if the written and the imprinted states are in opposite directions (e.g. up and down, respectively), the written (up) state will, as a function of time, show a tendency to revert to the imprinted (down) state, causing a ‘write’ error. If it is assumed that the capacitor is read non-destructively, the write error will be easily verified. However, if the capacitor is read destructively, the original state which had been written ‘up’ and subsequently imprinted to the ‘down’ state will correctly be read as a ‘down’ state, as long as the applied electric field is greater than the coercive field. If the applied field is less than the coercive field, the imprinted state will not switch, therefore causing an error. The process by which imprint manifests itself is via the reversal of ferroelectric domains (driven by the internal field generated by space charge, defect dipoles, charge at trap sites, or other mechanisms) [37]. The imprint effect is generally visualized through the shifts of hysteresis loops (Fig. 6).

In summary, both highly oriented and polycrystalline PZT-based capacitors with LSCO or hybrid LSCO-Pt electrodes fabricated on Si, using the PLAD method, exhibit excellent fatigue and retention characteristics at room temperature, demonstrating that it may not be absolutely necessary to have oriented PZT in order to achieve fatigue-free ferroelectric capacitors. In addition, PZT-based capacitors with LSCO or hybrid Pt-LSCO electrodes exhibit very small imprint and leakage current. These properties make these capacitors one of the two main candidates for application to the first generation of NVFRAM with PZT as the ferroelectric layer.

![Diagram](image)

Fig. 6. Schematic showing how imprint leads to asymmetric hysteresis loops along the voltage axes.
2.3.2. Processing–microstructure-property relationships of SBT films and integration with semiconductor substrates

Work on the synthesis and characterization of SBT thin films via a sol–gel process route demonstrated that the best ferroelectric properties were obtained for films that are non-stoichiometric (e.g. Sr_{0.8}Bi_{2.2}Ta_{2}O_{9}) [38]. More recently, pulsed laser deposition has been used to study both stoichiometry and process temperature effects on the synthesis of SBT films [39]. The work reported in [39] was focused on investigating the effect of Sr deficiency, where Sr was compensated by Bi atoms with a ratio of two Bi atoms to three Sr vacancies. The ceramic targets used to grow the films were prepared according to this overall stoichiometry, with additional 5% Bi excess to allow for Bi volatilization loss. Three different targets with controlled stoichiometry were used to grow SBT films, namely, SrBi_{2.1}Ta_{2}O_{9}, Sr_{0.7}Bi_{2.3}Ta_{2}O_{9}, and Sr_{0.55}Bi_{2.4}Ta_{2}O_{9}. SBT films were grown on Pt/ZrO_2/SiO_2/Si substrates at 650°C, via PLAD in 300 m Torr of oxygen. Films were annealed at 700, 750, and 800°C for 1 h in oxygen at atmospheric pressure. Patterned Pt top electrodes were produced at 400°C by IBSD and standard photolithography techniques followed by ion beam etching. Resultant top electrodes were 40 × 40 and 30 × 20 μm².

Fig. 7 shows XRD patterns for as-deposited and annealed SrBi_{2.1}Ta_{2}O_{9} films. The other SBT films indicated above revealed similar XRD patterns. These patterns reflect an increase in grain size or a decrease in inhomogenous strain resulting from annealing, which is manifested as a narrowing of the (1 1 5) SBT peak. Fig. 8 presents in greater detail the diffraction spectrum of Fig. 8 between 270 and 310 for the as-deposited SBT films of various compositions (Fig. 8(a)), and films annealed at 800°C (Fig. 8(b)). As-deposited films show an increased intensity of the 28.6° peak for compositions that diverge from the standard stoichiometry of SBT. This 28.6° peak may be assigned to the (0 0 8) SBT peak or the BiTaO₄(1 2 1) peak. The latter assignment is more likely since the intensity of the lower-angle peak increases with increased bismuth content. Upon annealing, these peaks collapse into a single peak closer to the (1 1 5) indexing that is expected for stoichiometric SBT films.

SEM and EDS analysis of as-deposited SBT films with the composition range described above show that as-deposited films have a fewer number of pinholes than those annealed at 800°C. In addition, the density of pinholes decreased as the Sr/Bi ratio increased. That is, the highest concentration of pinholes was observed in the films produced by ablation of the Sr_{0.55}Bi_{2.4}Ta_{2}O_{9} target. Films of this composition also contained many particles that appear to correlate with a Bi-rich second phase. However, these particles were found to be bismuth deficient when compared to the film composition as measured by EDS. One possible explanation for this phenomenon is that a

![Fig. 7. XRD pattern for pulsed laser ablation as-deposited SrBi_{2.1}Ta_{2}O_{9} and for films with subsequent annealing.](image-url)
Fig. 8. XRD spectrum of as-deposited (at 650°C) (a) and post-deposition annealed (at 800°C) (b) SBT films revealing the Sr/Bi ratio effect on the structure of the SBT films.

Bi-rich phase is formed during film deposition, but it decomposes during the post-growth anneal. Although this is consistent with the disappearance of the peak in the diffraction spectra tentatively assigned to BiTaO₄, more work is needed to establish the origin of this behavior. Other films with compositions nominally closer to stoichiometry did not exhibit such particles even when post-annealed.

Fig. 9 shows the stoichiometry dependence of hysteresis loops for SBT films after annealing at 750°C. The capacitor with the almost stoichiometric SBT layer exhibited the highest remnant polarization and the best-shaped loop. This was confirmed by measurements of the pulse switched polarization, \( P^r - P^\wedge \), which showed that \( P^r - P^\wedge \) values improve with increased post-SBT deposition annealing temperature. However, the values of polarization shown in Fig. 9 still are much lower that the highest values for SBT-based capacitors produced using MOD or MOCVD synthesis of SBT layers [40]. Further work on pulsed laser deposition of SET films is needed to clarify why the composition–microstructure–property relationships revealed for PLD SBT films are not equivalent to SET capacitors produced using other synthesis methods such as MOD and MOCVD.

2.4. Chemical vapor deposition and characterization of ferroelectric thin films

Of the variety of processing techniques for ferroelectric thin films, MOCVD offers the greatest potential advantages for application of ferroelectric materials to ULSI technologies, because of its
Fig. 9. Polarization hysteresis loops for SBT capacitors with different Sr/Bi ratio, for which the SBT films were annealed at 650°C. All measurements were taken at 5 V on 40 μm × 40 μm contacts.

well understood tool design, excellent film uniformity, compositional control, high film densities, high deposition rates, and amenability to large wafer-size scaling. Moreover, the need for a high degree of film thickness conformity over the complex device topographies common in ULSI circuits makes MOCVD one of the most appealing film synthesis methods. MOCVD is extensively utilized in many current commercial IC fabrication steps, and many equipment supplier are actively developing process tools for a variety of materials. Currently, a number of oxide ferroelectric thin-film materials [41–46] can now be routinely processed by MOCVD with quality approaching that of compound semiconductor films. In addition to ferroelectrics, a number of electrically conductive complex oxide thin films, critical for fabrication of PZT-based capacitors, have been successfully deposited by MOCVD (e.g. RuO₂) [47–50].

Despite the potential of MOCVD as an industrially viable process, large-scale utilization of these advanced thin-film materials presents significant processing challenges [51,52]. The primary factor limiting MOCVD of ferroelectric thin films arises from suitability of the current metal-organic precursors [53]. Efficient, reproducible MOCVD processes hinge critically upon the availability of high-purity metal-organic precursors with high and stable vapor pressures. A sufficiently high vapor pressure enables vapor-phase mixing of precursor components and transport of the reactants to the growing film. Adequate molecular stability of the precursor vapor is required to prevent premature reaction or decomposition of the precursor during vapor-phase transport. These qualities are often lacking in the currently available precursors needed for many ferroelectric materials. This has spurred the development of new chemical approaches to precursor design [53,54] and of alternative method of precursor vaporization and transport [46]. This section focuses on the synthesis of ferroelectric thin films by thermal MOCVD with emphasis on the choice of suitable precursor chemistries and new methods of precursor vaporization and transport. The synthesis of PZT films by thermal MOCVD is discussed as a prototypical system.

2.4.1. Standard precursor delivery techniques

Many of the standard design elements typical of thermal MQCVD are illustrated schematically in Fig. 10, which shows a cold-wall, horizontal flow design using a resistively-heated inconel
susceptor. The system is equipped with three liquid-source stainless steel bubblers containing the organometallic precursors for lead, titanium and zirconium. These bubblers are equipped with temperature and pressure regulation. The vapor-delivery-piping network is temperature regulated in order to prevent precursor vapor condensation that can lead to pipe clogging. Since the vapor pressure of most organometallic sources are non-linear functions of both temperature and pressure, a stable precursor vapor pressure is maintained using constant source temperature and source pressure. In this case, the precursor mass transport is directly proportional to the flow rate of the inert carrier gas through the source bubbler. This type of system design is typical of an MOCVD apparatus using liquid sources. For low-vapor-pressure, solid-source precursors, the traditional delivery technique of using direct sublimation of the solid or evaporation of the melt into the carrier gas flowing through a bubbler can also be used [47–50]. However, in this case, regulation of the bubbler pressure is rarely a benefit. For most deposition processes, the carrier gas is inert (e.g. He, N₂, Ar); however, active gases (e.g. NH₃) have occasionally been used to increase source vapor pressures [55–57].

As shown in Table 1, for many of the organometallic precursors used in growth of electroceramic films, sufficient vapor pressures (≥0.05 Torr) are obtainable only at elevated temperatures (typically 50–250°C) [58–60]. In order to prevent the condensation of precursors vapors in the delivery lines and clogging of the gas handling system, all portions of this network that transport chemical vapor must be heated to or above the evaporation temperature of the precursor. For some designs, parts of the deposition chamber will also require active heating to prevent condensation of precursors. In the case of PZT deposition using liquid sources, the source temperatures are moderate (~35–50°C), well below the thermal decomposition temperature of these compounds (~200°C). Consequently, only moderate heating of the gas-handling system (~60°C) is sufficient and a high degree of thermal uniformity is not critical. These requirements can be met by simply wrapping the delivery lines with electrically resistive heating tapes. By contrast, vapor delivery systems designed for the transport of many Ba or Sr precursors require heating to ~250°C to prevent condensation [53]. This temperature is sufficiently close to the decomposition temperature of
these sources that uniform heating of the gas-handling system is essential. In this case, the use of resistively heated lines is problematic since hot spots are very difficult to avoid. One elegant method to achieve this is to use a coaxial tubing design for the gas-handling system [61]. The inner tube transports the carrier gas and precursors vapor, while the outer tube flows hot oil to heat the inner tube. This design facilitates precise and uniform heating of the delivery lines, eliminating hot spots where the precursor could decompose prematurely. However, the use of liquid/gas heating in coaxial delivery lines is difficult and costly to implement for precursor delivery line networks that incorporate valves, manometers and pressure regulators [62].

For many material systems including electroceramic materials, thickness and compositional uniformity of the thin film is improved during MOCVD when processing occurs at reduced deposition chamber pressure (i.e. ≤100 Torr). Low-pressure operation improves the flow pattern of gas through the deposition chamber by minimizing the role of heat and flow instabilities caused by temperature gradients. In addition, low-pressure operation suppresses gas-phase pre-reactions by increasing the linear velocity of the process gases through the deposition chamber, thereby reducing the residence time of the gas mixture in the chamber [61].

2.4.2. Alternative precursor delivery techniques

Although many of the available precursors for electroceramic film growth have been successfully utilized to produce high quality ferroelectric films, significant deficiencies still exist with respect to the vapor pressure and vapor pressure stability of many of these compounds. This is especially true for the β-diketonate complexes of the alkaline earths (Ca, Sr, and Ba) [53,54]. In order to obtain adequate mass transport using a conventional bubbler delivery line, the low vapor pressure of these compounds necessitates high source temperatures. At these elevated temperatures, these precursors are chemically unstable and they gradually decompose [53,54]. Consequently, the

<table>
<thead>
<tr>
<th>Compound</th>
<th>Phase</th>
<th>Melting point (°C)</th>
<th>Vapor pressure (Torr)</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ba(TMHD)$_2$</td>
<td>Solid</td>
<td>194–197</td>
<td>0.05</td>
<td>200</td>
</tr>
<tr>
<td>Bi(TMHD)$_3$</td>
<td>Solid</td>
<td>114–116</td>
<td>0.05</td>
<td>150</td>
</tr>
<tr>
<td>(C$_2$H$_4$)$_2$Bi</td>
<td>Solid</td>
<td>77–78</td>
<td>0.20</td>
<td>100</td>
</tr>
<tr>
<td>(CH$_3$)$_3$Bi</td>
<td>Liquid</td>
<td>−107.7</td>
<td>9.50</td>
<td>0</td>
</tr>
<tr>
<td>La(TMHD)$_3$</td>
<td>Solid</td>
<td>227–231</td>
<td>0.20</td>
<td>210</td>
</tr>
<tr>
<td>(C$_2$H$_4$)$_2$Mg</td>
<td>Solid</td>
<td>176</td>
<td>0.10</td>
<td>160</td>
</tr>
<tr>
<td>Mg(TMHD)$_2$</td>
<td>Solid</td>
<td>135–150</td>
<td>0.05</td>
<td>150</td>
</tr>
<tr>
<td>(C$_2$H$_4$)$_2$Pb</td>
<td>Liquid</td>
<td>−136</td>
<td>2.00</td>
<td>50</td>
</tr>
<tr>
<td>Pb(TMHD)$_2$</td>
<td>Solid</td>
<td>126–128</td>
<td>0.05</td>
<td>180</td>
</tr>
<tr>
<td>(C$_2$H$_4$)$_2$Pb</td>
<td>Solid</td>
<td>229–230</td>
<td>0.05</td>
<td>230</td>
</tr>
<tr>
<td>Nb(OC$_2$H$_5$)$_3$</td>
<td>Liquid</td>
<td>6</td>
<td>0.10</td>
<td>142</td>
</tr>
<tr>
<td>Ru(TMHD)$_3$</td>
<td>Solid</td>
<td>120–125</td>
<td>0.50</td>
<td>120</td>
</tr>
<tr>
<td>(C$_2$H$_4$)$_2$Ru</td>
<td>Solid</td>
<td>194–198</td>
<td>0.10</td>
<td>190</td>
</tr>
<tr>
<td>Sr(TMHD)$_2$</td>
<td>Solid</td>
<td>125</td>
<td>0.30</td>
<td>230</td>
</tr>
<tr>
<td>Ta(OC$_2$H$_5$)$_5$</td>
<td>Liquid</td>
<td>21</td>
<td>0.10</td>
<td>140</td>
</tr>
<tr>
<td>Sn(OC(CH$_3$)$_2$)$_4$</td>
<td>Liquid</td>
<td>45</td>
<td>0.30</td>
<td>65</td>
</tr>
<tr>
<td>(C$_2$H$_4$)$_2$Sn</td>
<td>Liquid</td>
<td>−112</td>
<td>10.0</td>
<td>145</td>
</tr>
<tr>
<td>Ti[OC(CHOH)$_2$CO]$_4$</td>
<td>Liquid</td>
<td>19</td>
<td>5.00</td>
<td>92</td>
</tr>
<tr>
<td>Ti[OC(CHOH)$_2$]$_4$</td>
<td>Liquid</td>
<td>0.20</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>Ti[OC(CHOH)$_2$]$_2$(TMD)$_2$</td>
<td>Solid</td>
<td>220</td>
<td>1.00</td>
<td>240</td>
</tr>
<tr>
<td>Zr[OC(CHOH)$_2$]$_4$</td>
<td>Liquid</td>
<td>1.00</td>
<td>65</td>
<td></td>
</tr>
<tr>
<td>Zr(TMHD)$_4$</td>
<td>Solid</td>
<td>308</td>
<td>0.10</td>
<td>180</td>
</tr>
</tbody>
</table>
vapor pressure of these compound decreases as a function of time, detrimentally affecting film-growth reproducibility. In order to circumvent these problems, alternative methods of precursor delivery and vaporization have been developed.

One of the most promising methods of alternative precursor delivery is known as liquid delivery or liquid-source injection [46,63]. In this process, the low-vapor-pressure solid precursor is dissolved with an organic solvent to form a solution [63]. These systems operate by introducing liquids or mixtures of liquids at high pressure into a point-of-use hot vaporization cell. There, the solution is flash evaporated and introduced as either net (100% precursor) vapor or vapor diluted with a carrier gas into the MOCVD deposition chamber. Often, the vaporization cell is installed directly onto the deposition chamber’s vapor inlet to reduce the required residence time in the piping network, thus minimizing the opportunity for premature decomposition. This delivery technique is compatible with both atmospheric- and low-pressure MOCVD applications, and process tools of this type, incorporating up to four liquid-sources reservoirs, are now commercially available.¹ These systems are particularly well suited for the processing of multicomponent systems, where flows from the individual reservoirs must be precisely metered and mixed. Thus, by using a separate elemental precursor solution per reservoir, stoichiometric vapor can be generated. Alternatively, the individual precursor component solutions may be mixed stoichiometrically into single solution in one reservoir. A third option, that is particularly useful for ferroelectric films, is to use multiple reservoirs, each containing different mixed precursor solutions. For example, for processing of BST, separate reservoirs containing premixed stoichiometric solutions for BaTiO₃ and SrTiO₃ can be used to produce a quasi-two-component source chemistry that spans the entire BST phase diagram.

A second alternative delivery method, referred to as solid-source delivery, takes advantage of the long-term instability of some of the β-diketonates at high source temperature. For short-term high-temperature exposure, the compounds have adequate chemical stability to exhibit reproducible vapor pressures characteristics. In this vaporization approach, only sufficient precursor material to sustain constant mass transport is exposed to the high thermal load required for vaporization [64]. A single solid-state precursor compound or a mixture of these compounds is fed into a high-temperature-gradient vaporization zone. The temperature gradient is sufficiently broad, so that each precursor component vaporizes in this zone at its own specific vaporization temperature. Once the vapor is formed, it is immediately swept to the deposition chamber by a flow of inert carrier gas. Unlike conventional liquid-source bubbler delivery, the rate of mass transport is largely independent of the carrier-gas flow rate and is determined primarily by the rate at which the solid precursor is metered into the hot vaporization zone. Multicomponent precursor vapors are produced either using multiple solid-source delivery lines, each feeding a single precursor compound at a different metering rate, or by using a single solid-source delivery line feeding a single powder containing the appropriate mixture of solid-state precursors required to produce the desired stoichiometric ratio [64]. Ideally, all the solid-state source fed into the zone should vaporize completely leaving no residue. Once the vapor is generated, the considerations and requirements for the transport of the vapor to the deposition chamber are the same as in conventional liquid-source delivery as discussed above. This type of delivery line can be connected to any conventional MOCVD deposition chamber.

For multicomponent films, two difficulties limit the robustness of this method. First, the precursor powders must be uniformly and reproducibly packed into the feed tube of the delivery line. For multicomponent powders, the constituents must also be homogeneously mixed. This can be a non-trivial process since the grain size and propensity for agglomeration of a given powder can vary.

¹ATMI (Danbury, CT) and MKS Instruments Inc. (Danvers, MA) are two companies which currently manufacture liquid-source delivery systems.
between compounds, vendors and batches. Second, in the case of mixed powders, substantial differences in ligand chemistry, vaporization temperature, or decomposition characteristics between the constituent components can lead to non-volatile reaction products, unvaporized precursor powder, or decomposition residues, respectively, remaining in the fed tube. These effects compromise the control and reproducibility of film stoichiometry. By using single ligand chemistry for all mixed-source constituents (i.e. β-diketonates), these effects can be reduced; however, substantial differences in volatility can still lead to problems. For example, SrRuO$_3$ films grown by solid-source delivery, we have found that stoichiometric films can only be produced using a Sr-rich precursor mixture (Sr:Ru 1.7:1), due to the much lower vapor pressure of Sr(TMHD)$_2$ compared to that of Ru(TMHD)$_3$ (see Table 1).

As an example of the quality of ferroelectric films that can be produced by MOCVD, we discuss some of our efforts in the deposition of epitaxial PZT thin films by conventional thermal MOCVD. The high quality of these materials is illustrated in TEM analysis for tetragonal samples that shows that the films are epitaxial and single-crystal. The primary structural defects are 90° domains and threading dislocations [43,44]. This is clear from the cross-sectional TEM image of a PbTiO$_3$(0 0 1)/SrRuO$_3$(1 0 0)/SrTiO$_3$(1 0 0) epitaxial film shown in Fig. 11. Fig. 12 shows the ferroelectric hysteresis loops for capacitors formed from epitaxial Pb(Zr$_x$Ti$_{1-x}$)O$_3$/SrRuO$_3$(0 0 1)/SrTiO$_3$(0 0 1) thin films of various compositions: (a) $x = 0.35$; (b) $x = 0.40$ (tetragonal compositions); (c) $x = 0.56$ and (d) $x = 0.70$ (rhombohedral compositions) using Ag top electrodes [49]. The loops show that the films exhibit excellent ferroelectric behavior as indicated by square-shape of the loops with large spontaneous polarizations ($P_s$) and low coercive fields ($E_c$). For $x < 0.30$ and $x > 0.80$, open-shaped ferroelectric hysteresis loops were observed due to high leakage currents. For $0.30 < x < 0.80$, the $P_s$ values were in the range of 32–55 mC cm$^{-2}$ and showed a clear dependence on $x$ with a minimum near the morphotropic boundary. These values of $P_s$ and the dependence of $P_s$ on composition are quite different from that of bulk PZT ceramics [65], where $P_s$ exhibits a maximum at the morphotropic phase boundary [66–68]. This difference arises since the value of $P_s$ obtained in PZT

![90° Domain Threading Disl](image)

**Fig. 11.** Cross-sectional TEM image of an epitaxial PbTiO$_3$(0 0 1)/SrRuO$_3$(1 0 0)/SrTiO$_3$(1 0 0) thin film. The interfaces are atomically sharp, and the dominant structural defects in the film are 90° domains and threading dislocations.
Fig. 12. Ferroelectric hysteresis loops for various compositions of epitaxial PZT thin films grown at 700°C on epitaxial SrRuO$_3$(0 0 1) buffered SrTiO$_3$(0 0 1) substrates: (a) $x = 0.35$; (b) $x = 0.40$ (tetragonal structured); (c) $x = 0.56$ and (d) $x = 0.70$ (rhombohedral structured).

ceramics depends primarily on the ease with which the sample can be poled and not on the intrinsic single crystal value of $P_r$. The $E_c$ values exhibited a steep decline with increasing $x$, from 76 to 21.5 kV cm$^{-1}$ at $x = 0.30$ and 0.80, respectively. These values of $E_c$ are considerably higher than that of PZT ceramics (∼5–20 kV cm$^{-1}$) [64] probably due to piezoelectric effects caused by the mechanical constrain of the substrate. However, the $E_c$ values are significantly lower than most reported values of $E_c$ for PZT films [66–68].

All compositions showed high fatigue resistance with the lowest fatigue rate occurring for the $x = 0.40$ composition that retained 96% of the initial $P_r$ after $2 \times 10^8$ cycles. However, we could not infer any compositional dependence of the ferroelectric fatigue from our data. The relative dielectric constant (at 1 kHz) as a function of composition exhibits a peak near the morphotropic boundary similar to bulk ceramics [69]. The dielectric loss, tan $\delta$, was above 0.10 for $x < 0.20$. However, for $x \geq 0.20$, tan $\delta$ was 0.015–0.04. For $x \geq 0.20$, the films were good insulators, typically displaying electrical resistivities, $\rho$, in the range of $10^{12}$–$10^{14}$ Ω cm with breakdown strengths of 300–700 kV cm$^{-1}$ [62].

In summary, the processing of PZT films by thermal MOCVD was discussed as a prototypical system with special emphasis on the choice of suitable precursor chemistries, and new methods of precursor vaporization and transport. Despite considerable progress, further efforts are needed to
improve precursor characteristics (e.g. reactivity, vapor pressure, vapor pressure stability, synthesis scaling, and environmental compliance) through chemical modification, particularly for alkaline earth precursors. In addition, promising new developments in alternative precursor vaporization and vapor delivery methods were discussed. Coupled together, further advances in these areas could provide the precise control of film stoichiometry that will lead to the scaleable and robust MOCVD processes, which is a requisite for a successful ULSI process for these thin film materials.

3. Integration on Si for NVFRAM

3.1. From epitaxial to polycrystalline PZT films and the route to a manufacturable process

Imagine for a moment that your are the lead process engineer with the responsibility of coming up with the most optimized route to manufacture NVFRAM based on PZT films. You now have the job of identifying the various processing steps that will go into making this happen, including the tools required to deposit and etch and connect the various layers in the memory cell. Note that all the steps have to be manufacturable (i.e. they should be scaleable to larger wafers, should have as little as possible defects, should have high throughput and should be high-yield processes). In this section we will take the reader through an actual process integration scheme in which LSCO/PZT/LSCO capacitors are integrated onto a Si-CMOS wafer to fabricate memory cells [70]. Most likely, the ferroelectric layers will be deposited onto a Si wafer in which the CMOS processing is already completed. Such a process route is called back-end processing, which has the advantage that the wafers do not go back into the Si processing fab-line after the ferroelectric layers are deposited (to avoid contamination).

Fig. 13 shows a typical process flow that will yield ferroelectric capacitors on a filled poly-Si plug. Fig. 13(a) is where you start the back-end processing by depositing the conducting barrier layers (for example, TiN/Pt) on the poly-Si plug. This is followed by the deposition of the bottom electrode, which in our case is LSCO. This layer is deposited by sputtering at room temperature followed by an annealing treatment at elevated temperatures (600–650°C, in air) and it is polycrystalline. Manufacturable deposition processes for the LSCO layer are readily available, among which sputtering and chemical vapor deposition have yielded high quality LSCO layers. At this stage, the bottom electrode size is defined by the first level mask and etching (Fig. 13(b)). Although this article will not delve into the details of the etching protocols and the various types of etching processes, it suffices to say that a dry etching protocol is a crucial component of manufacturable process [71]. Typically, reactive ion etching (RIE) is the most desirable etch process, since it has very high degree of etch selectivity, very little damage and good side wall definition, all of which are critical to successfully define a high density memory element. RIE of these multicomponent oxides is in its infancy and further work needs to be done. After the definition of the bottom electrode, a diffusion barrier (in this case TiO₂) is deposited to prevent: (i) electrical contact of the top and bottom electrode layers and (ii) chemical reaction between the PZT and the field oxide (SiO₂). Then, the ferroelectric layer is deposited (in this case by sol–gel processing sputtering or chemical vapor deposition), followed by the top electrode layer (in this case LSCO/Pt) and the interlevel dielectric (also known as the passivation layer). The second mask level at this stage defines the overall capacitor structure (Fig. 13(c)) and again involves RIE down to the TiO₂ barrier layer. Finally, the third mask is used to open up a via in the interlevel dielectric to make metal contact to the top electrode. Fig. 13(d) shows the final finished capacitor. The top metal contact involves sputter or e-beam deposition followed by a sintering treatment in nitrogen at about 450°C.
Although the above paragraph provides a very simplified and (apparently easy) view of a full-scale process integration, in reality, a whole host of problems may arise and have to be solved. Process damage, for example, is possibly the most important issue. For example, one might obtain very desirable ferroelectric properties in capacitors that are delineated by lift-off processes (i.e. the capacitor stack is not fabricated by a dry etch process); however, when the same capacitors are fabricated by a process similar to that described in Fig. 13 (i.e. involving full-wafer lithography and dry etching), there is a strong possibility that the ferroelectric properties are either diminished or in some cases, even destroyed. In general, electrical measurements are the best indicators of possible process damage. For example, ion beam damage during etching can lead to shifted or distorted hysteresis loops. Fig. 14 shows hysteresis loops measured at three different stages during the process flow and illustrates the robustness of this process flow. These integrated capacitors can be used to probe the properties under environments approximating those in an actual memory cell.

We now describe some of the key measurements that can be made with such integrated capacitors. Of course, one can measure the hysteresis loops (as in Fig. 14), which is typically obtained under quasi-static test conditions. However, such measurements are not directly relevant to a memory environment, where short pulses are used to write and read the memory states. Therefore, the ferroelectric capacitors have to be characterized using such short pulses, thus leading to dynamic
Fig. 14. Polarization hysteresis loops measured at the different stages during the process flow.

responses. Fig. 15(a) shows the circuit diagram that is typically used to carry out pulsed testing. In order to fully characterize the ferroelectric responses and correlate to logic ‘1’ and ‘0’ states, typically a set of two measurements are carried out, which we have described earlier as $P^*$ (switched polarization, corresponding to logic ‘1’) and $P^\wedge$ (non-switched polarization corresponding to logic ‘0’). The current responses corresponding to these two are shown in Fig. 15(b) along with the difference ($\Delta P = P^* - P^\wedge$). The integral of $\Delta P$ over the entire switching time gives the total charge switched.

How does one understand polarization dynamics from such data? The early work of Merz and others [72–81] provides an approach to understand the switching transients. This is illustrated in Fig. 15(c) for the data from the integrated test capacitors. The Merz model correlates the maximum switching current $i_{\text{max}}$ and the switching time $t_s$ to the applied field through an exponential relationship (see inset in Fig. 15(d)) involving a parameter termed the activation field. The activation field, obtained from the slope of the straight line fit, is the equivalent of the coercive field (which is the average switching field under quasi-static conditions), when the capacitor is tested under pulsing conditions; it provides a quantitative measure of the energy required to switch the polarization. On the other hand, the switching time $t_s$ provides a measure of the dynamics of the switching process; however, it is a very difficult quantity to measure.
Fig. 15. (a) Schematic of the electrical circuit used for measuring switching current responses; (b) current response corresponding to switched, non-switched and remnant polarization for a typical PNZT capacitor with LSCO electrodes; (c) typical switching current responses for a LSCO/PNZT/LSCO capacitor at different applied electrical fields; (d) the maximum switching current, \(i_{\text{max}}\) as a function of reciprocal pulse voltage applied to the capacitor.

An important question arises: how sensitive is the activation field to circuit parameters such as the load resistance/capacitance, parasitics, equipment limitations such as the rise time of the oscilloscope and the pulse generator? All these parameters definitely affect the measurement of the switching time and this leads to a strong uncertainty in measuring this quantity. However, as shown in Fig. 16, they do not influence the activation field appreciably. The data shown in Fig. 16 were obtained for capacitors of different sizes (i.e. the load capacitance is different) as a function of the load resistance in the circuit \([82,83]\). We note that the switching time, which is of the order of 15 ns (from Fig. 15(b)), is still much higher than that expected from theoretical predictions (theory suggests an intrinsic switching time of the order of a few hundred picoseconds). More recently, we have measured the switching properties of the same capacitors using an optical–electrical measurement set-up and have obtained essentially the same value of activation field, but with an experimentally measured switching time of the order of 5 ns. This set-up uses a femtosecond optical pulse to trigger an electrical pulse generator that subsequently applies the test pulse to the capacitor.

Consistent with measurements on capacitors that have not experienced this level of integration, these capacitors do not show appreciable fatigue or retention loss; therefore we do not elaborate on these device properties any further. Imprint is an issue that is being addressed in great detail by several research groups. In simple terms, imprint is the development of an internal field in the capacitor and manifests itself as a progressive shift of the hysteresis loop along the field axis. Why is this important? To put this in perspective, one needs to understand some of the potential application
markets of ferroelectric memories. Among them, the erasable programmable read-only memory (EPROM) and the electrically erasable programmable read-only memory (EEPROM) markets are prime targets, since they are also non-volatile memories, but have limited number of write operations. An EPROM is typically used in a write once and read many times mode. For example, the memory could be programmed into one logic-state, which could subsequently be read a few million times. Since the read process involves the application of a pulse of the same polarity, the storage element will repeatedly see voltage pulses of the same polarity, i.e. it effectively sees do field. Translate this to a ferroelectric memory: the ferroelectric capacitor, used under these conditions, will experience repeated unipolar pulses. Under these read conditions, there exists strong possibility for charged defects in the capacitor to transport across the capacitor, segregate a one of the electrode–ferroelectric interfaces and create an internal field. This internal field shows up as a shift of the loop along the field axis and in pulsed polarization measurements as $P^\ast - | - P^\ast |$ or $P^\ast - | - P^\ast |$ tending to zero [84]. Imprint failure occurs when one of the coercive fields goes to zero (i.e. one polarization state becomes unstable and reverts to the opposite state). In terms of pulse polarization, this happens when $P^* = | - P^\ast |$ or $P^\ast = | - P^\ast |$. The formation of this internal field can happen with or without the assistance of temperature. In general, tests to study imprint are carried out under two conditions: (i) static imprint, in which the sample is put into a polarization state and the heated to the desired temperature (for example, 100°C) and held for a fixed period of time (e.g. 1 h). Imprint stress in this case is purely thermal; (ii) dynamic imprint in which single-sided pulses (or a dc field) are imposed on the capacitor in addition to the thermal stress. Resistance to the development of such an internal field is an important requirement in ferroelectric memories.

The normalized voltage shift in the loop can be computed by averaging the negative and positive coercive voltages with respect to the initial coercive voltages. Initial asymmetry (if any) is taken into account in calculating the figure of merit (FOM) [84].

$$FOM1 = V_c^{\text{shift}} = \frac{(+V_c^{\text{final}}) + (-V_c^{\text{final}})}{(+V_c^{\text{initial}}) - (-V_c^{\text{initial}})}$$

where $V_c^{\text{shift}} = \pm 1$ would be the imprint failure condition, indicating a complete shift. A directly observable consequence of any asymmetry is the larger switching voltage needed to switch to one of
Fig. 17. Dynamic imprint behavior for LSCO/PZT/LSCO capacitors, showing negligible imprint as required for commercial NVFRAM: (a) imprint figures of merit for capacitors of different area; (b) imprint figures of merit as a function of number of unipolar pulses at 100°C.

the polarization states compared to the other. A second FOM to quantify imprint, FOM2 is based on the polarization values and is defined as $2.5/(P_{f}^{r} - | - P_{f}^{\lambda}|)$. In this case, $P_{f}^{r}$ is the switched polarization value of the original state, while $| - P_{f}^{\lambda}|$ is the unswitched polarization value for the imprinted state (or the preferred state). FOM2 attaining a value of one would be the failure condition. Unlike FOM1, the difference in the polarization values are directly related to memory operation since the retained polarization constitutes the signal available for sensing the logic state. By this standard, when $(P_{f}^{r} - | - P_{f}^{\lambda}|) \leq 2.5 \mu C cm^{-2}$ (by device specifications), the capacitor is said to have undergone an imprint failure, since this effectively means that the sense amplifier can no longer distinguish between the written state and its complementary state.

As mentioned earlier, due to defects introduced during processing the imprint behavior for smaller area capacitors could be different. This is an important consideration since the actual high-density memory technology will use capacitors with lateral dimensions of the order of a micron. The fabrication of such small capacitors using dry etching techniques could very likely lead to defects such as surface amorphous layers, defects that can act as trap sites, etc. Fig. 17(a) plots the imprint test results for capacitors of different areas ranging from 100 $\mu m \times 100 \mu m$ to 6 $\mu m \times 6 \mu m$. Notice that the imprint properties of the capacitors as measured by the two FOM's do not change appreciably as the area is reduced. Fig. 17(b) plots the imprint results of capacitors subjected to different number of $+5 \ \text{V}$ unipolar pulses at 100°C. The cumulative nature of the imprint process is clearly evident from this data. Our capacitors showed negligible imprint up to $10^{10}$ cycles.

The physical mechanism of imprint or the development of the internal field in thin film ferroelectrics is yet to be established. In addition, the role of process variables [85], defects, and the stressing conditions needs to be fully understood. In order to understand this, it is essential to examine the nature of defects in the ferroelectric film and the electrode layers and how they interact with the switching process. For example, oxygen vacancies and lead vacancies in PZT are known to influence the reliability of such devices. These defects can form dipoles or interact with the domain and adversely affect the properties of the capacitor. Alternatively, these defects can lead to a space charge formation at the interface, which can play an important role in the switching behavior of the ferroelectric capacitor. Especially, at higher voltages charge being injected into the electrode may exceed the charge being transported through the film and a space charge may start developing at the interfaces with time. This interface charge could be pinning the dipoles, which is observed as a loss
of switched polarization for one state (see Fig. 18(a)). The schematic shown in Fig. 18(b) illustrates the dipole/domain pinning phenomenon at higher applied voltages. Domain pinning within the bulk of the ferroelectric can also be expected by the electrons released from their trapping centers at high temperatures and large fields as discussed earlier.

Another processing-related concern in Si technology is the presence of interface-trapped charges, which have energy states in the forbidden band gap and can interact electrically with the underlying silicon [86]. A low temperature forming gas (hydrogen containing gas) anneal at \( \sim 400^\circ\text{C} \) ties up dangling bonds at the Si/SiO\(_2\) interface, thus reducing trap sites. Unfortunately, both Pb(Zr, Ti)O\(_3\) and SrBi\(_2\)Ta\(_2\)O\(_9\) ferroelectric thin film capacitors lose their polarization hysteresis characteristics as a result of such an anneal [87–89]. The degradation of ferroelectric properties has been correlated with the top electrode [87–89]. Ferroelectric capacitors with In\(_2\)O\(_3\) top electrode showed least amount of degradation when subjected to forming gas anneal. In contrast, it was determined that Pt is the worst electrode [89]. This has been attributed to the catalytic nature of Pt in dissociating the hydrogen molecule into atoms.

For example, Fig. 19 plots the polarization–voltage hysteresis loops for Pt/PZT/Pt capacitors before and after forming gas anneal performed at temperatures between 200 and \( 400^\circ\text{C} \). Prior to the forming gas anneals, the capacitors show S-shaped hysteresis loops with saturation at 5 V and coercive field of \( \sim 1 \) V. After forming gas anneal, the capacitors are no longer ferroelectric. Notice that even the sample annealed at \( 200^\circ\text{C} \) is no longer switching. The inset shows the change in the resistivity of the capacitors as the temperature of the forming gas anneal is increased from 200 to \( 400^\circ\text{C} \). The resistivity drops from \( \sim 5 \times 10^{11} \) \( \Omega \) cm for the as-grown capacitor to \( \sim 2 \times 10^7 \) \( \Omega \) cm for a film annealed in forming gas at \( 400^\circ\text{C} \) for 30 min. The change in resistivity of the films could be due to any one or more of the following reasons. Since forming gas (4% H\(_2\)/balance N\(_2\)) creates a reducing ambient (\( p_{\text{O}_2} \sim 10^{-20} \) bar), oxygen may be lost from the PZT film, thereby creating free electrons, which will increase its conductivity. However, another possible scenario is the incorporation of hydrogen into the PZT lattice. Hydrogen upon ionization would release electrons, which would also lower the resistivity of the films. Moreover, hydrogen can interact with an oxygen ion to form a polar hydroxyl ion. All the scenarios discussed above can simultaneously or individually lead to the degradation of the ferroelectric properties [90,91].

Fig. 20 shows the Raman spectra for epitaxial PZT/LSCO and LSCO films after forming gas anneal at \( 450^\circ\text{C} \) for 30 min. This spectrum clearly demonstrates that the Raman features observed
are only from the PZT film. The lines in the figure show the peak positions of the PZT film before forming gas anneal. The inset of Fig. 20 shows the Raman spectra in the high frequency regime for the films. There is a mode at ~3700 cm\(^{-1}\) in the annealed film, which corresponds to a polar hydroxyl [OH\(^{-}\)] bond stretching [92]. This feature is absent in the as-grown PZT film, indicating that hydrogen is incorporated in the film during forming-gas annealing. Infrared absorption bands due to O–H vibration in a similar wave-number range have been reported in other perovskite-type crystals as well such as SrTiO\(_3\) [92]. In forming gas annealed PZT films, oxygen can be lost and the formation of [OH\(^{-}\)] bonds can cause anti-symmetric stretching of the O–Ti–O bonds. Further work is needed to comprehensively understand the Raman results.

Fig. 20. Raman spectra for epitaxial PZT films deposited on LaAlO\(_3\)(0 0 1) substrates with a LSCO bottom electrode before and after forming gas anneal at 450°C for 30 min. Inset shows the Raman spectra for the films at higher wave-numbers.
Based on the Raman data and simulations from NEC [93], possible locations of the hydrogen ion and how it is responsible for the degradation of the ferroelectric properties are discussed. Fig. 21 is a schematic showing four possible positions for hydrogen in the PZT. Since the site between the Ti and planar O ions, and the site between the two Pb ions would contribute bending vibrations (which are absent in the Raman spectra), these sites are unlikely to be occupied. This leaves the possibility that hydrogen occupies the tetrahedral sites or the site between the apical oxygen ions and Ti. An earlier study has also predicted similar positions for hydrogen ions in SrTiO₃ crystals [92]. However, it is not clear how hydrogen in the tetrahedral sites would affect the out of plane polarization. This implies that only the apical oxygen ions form the polar hydroxyl ion. The Raman data in conjunction with the electrical data suggests that the hydrogen ions bond with one of the apical oxygen ions to form a polar hydroxyl ion.

Although the degradation mechanisms are not yet understood, it is clear that these devices must be protected against oxygen loss and hydrogen incorporation during forming gas annealing. Since forming gas anneals are done to tie up dangling bonds at the Si/SiO₂ interface, it is not possible to restore the oxygen lost and therefore its loss must be prevented. However, if the process of hydrogen incorporation is reversible, it may be removed from the memory device by post annealing in non-oxygen ambient. Unfortunately, hydrogen damage of Pt/SrBi₂Ta₂O₉/Pt capacitors is irreversible. Our studies on PNZT capacitors with LSCO electrodes show that hydrogen damage is reversible.

Fig. 22 plots the hysteresis loops measured before forming gas annealing and the inset shows the polarization–voltage curve after forming gas annealing for fully integrated devices using ~65 nm La₀.₅Sr₀.₃CoO₃ (LSCO) electrodes, ~200 nm Pb Nb₀.₀₄Zr₀.₂₈Ti₀.₆₆O₃ (PNZT) as the ferroelectric and TiOₓ and SiO₂ as the interlevel dielectric layers. This capacitor structure was annealed in forming gas at 400°C for 30 min. After annealing in forming gas, the capacitors become less resistive due to hydrogen incorporation. The interlevel dielectric layers, TiOₓ and SiO₂ effective barriers to oxygen and PbO loss (due to low diffusivities) from our capacitors. Since post anneals cannot be performed in oxygen ambient, we annealed the capacitor structure in flowing VLSI grade N₂, which has oxygen and hydrogen impurities of less than 1 ppm. The post-annealing temperature was above the Curie temperature, θc for various time periods till the capacitors recovered their original resistivity and polarization. Also plotted in Fig. 22 are the hysteresis loops for the capacitors annealed at 400°C in VLSI grade N₂ for 30 min and 4 h. After 30 min the capacitor has partially recovered. The capacitor
recovered some more after a total of 90 min and completely recovered after 4 h. Annealing the forming gas treated capacitors in VLSI grade N₂, creates a chemical potential gradient for hydrogen due to its low chemical activity in the ambient as opposed to the ferroelectric capacitor. Since hydrogen is likely to be mobile at the post-annealing temperature of 400°C, it can diffuse out of the capacitor structure [90,91].

The recovery time of the capacitor is determined by the mobility and the activity of hydrogen at the anneal temperature. The mobility of hydrogen can be increased by increasing the post-anneal temperature. The recovery anneal time reduces to 30 min by increasing the post-anneal temperature to 500°C as opposed to 4 h at 400°C for capacitors that were annealed for 30 min in forming gas at 400°C. To change the activity of hydrogen in the capacitors after forming gas annealing, the fraction of hydrogen in the forming gas mixture was reduced from 4 to 1 and 0.5%. Clearly, the extent of damage to the capacitor should depend on the amount of hydrogen incorporated into the lattice during forming gas anneal. Consistent with the lower amounts of hydrogen diffusing into the capacitor structure, the recovery time at 400°C was found to decrease to 15 min for 0.5% H₂ and 30 min for 1% H₂ in the forming gas mixture.

To trace the hydrogen, we have also performed Raman scattering experiments. Fig. 23 shows the Raman spectra in the high frequency regime for epitaxial PNZT/LSCO/LaAlO₃ before forming gas anneal, after forming gas at 450°C for 30 min, and after annealing the forming gas exposed PNZT in VLSI N₂. The mode at ~3700 cm⁻¹ in the forming gas annealed film corresponds to a polar hydroxyl [OH⁻] bond stretching and is formed due to the incorporation of hydrogen during forming gas annealing. Fig. 23 shows that the [OH⁻] stretching vibration mode appears only after forming gas annealing. This mode becomes much broader and diffuse with a significantly reduced intensity in the film after annealing in VLSI N₂ for 4 h, indicating that the hydrogen was successfully removed from the lattice. The electrical data in conjunction with Raman data clearly demonstrate that the recovery of ferroelectric properties is directly related to the removal of hydrogen from the capacitor structure. In summary, the chemical potential difference of hydrogen between a forming gas annealed capacitor and the ambient can be successfully used to diffuse the hydrogen out of the films.
3.2. Stacked cell processing issues

As one progresses from the low density architecture described above to a high density, vertically integrated architecture, the level of complexity in design and materials integration becomes much higher. Fig. 24 shows schematically the memory cell architecture of stacked cells in 0.35–0.13 \( \mu \text{m} \) generations in which the ferroelectric capacitor is located directly on top of the pass-gate transistor. We focus on one specific issue, namely, the materials science of conducting barrier layers between the bottom electrode and the poly-Si plug. Before we do this, some of the key issues relevant to the manufacturability of such a high density memory are outlined below.

These issues (many of which are also relevant to the low density, memory architectures) can be summarized as follows.

1. Use of chemical mechanical polishing for planarization of the interlevel dielectric.
2. Use of a barrier metal to stop oxygen ions from diffusing and oxidizing the drain plug just below the ferro-capacitor bottom electrode. This creates a low dielectric constant parasitic capacitor, which can absorb most of the potential drop when voltage is applied to read or write into the ferroelectric capacitor.

Fig. 24. Cell architecture of a high density NVFRAM.
3. Use of ferroelectric films of thickness $\leq 100$ nm. Conformal deposition over bottom electrode is necessary.
4. Use of a capping layer to reduce $H_2$ degradation of the ferroelectric oxide stoichiometry (not to exceed 25 nm), which was discussed above.
5. Use of Pt electrode to make an electrical connection with the Al interconnect buffer layer.
6. Use of low thermal budget annealing of the ferroelectric film. Temperature of 700$^\circ$C or less are preferred (RTO at 700$^\circ$C, and RTA (inert) at even low temperature).
7. Etching of the bottom electrode and the overall capacitor stack without sidewall degradation of the ferroelectric film.

These seven issues need to be optimized in order to produce a capacitor with the following characteristics.

1. Leakage below $1 \times 10^{-8}$ A cm$^{-2}$.
2. Fully saturated loops at 1.5 V away from the edge of the Q versus V plot.
3. No appreciable fatigue $\geq 10^{12}$ polarization switching cycles (for thin-films less than 100 nm and with fields as high as 250 KV cm$^{-1}$).
4. Less than 4% imprint at 85$^\circ$C after $10^9$ unipolar disturbs. All measurements (store, stress and probing at the opposite state) at the elevated temperature.
5. The $2P_r$ greater than 15 $\mu$C cm$^{-2}$ at the end of the encapsulation.
6. The $\Delta (2P_r)$ during processing to be nearly zero. This means that starting with high $2P_r$ and degrading over the process history of the integration scheme is not acceptable. Deterioration of $2P_r$ shows intrinsic lack of stability of the capacitor material/electrodes and will lead to imprint, fatigue and leakage. Designing wide margin sense amps to circumvent, this is possible in low density devices, but not in advanced high-density generations. The thinner the film, the more prone to deterioration it is. This is particularly more stringent in 1 T–1 C schemes.
7. If issues 1–6 can be achieved, time-dependent-dielectric-breakdown (TDDB) may follow. Typical 10 years and TDDB must be achieved.

Once an optimized capacitor process is achieved, device models and reliability models can be used to track these parameters and provide memory designers with a design window. These models are necessary for the extreme cases of thickness scaling below 100 nm. In such a situation, process control is very severe and variations in stoichiometry and microstructure can lead to a never-ending search for respectable results that may never come. Among the many materials related issues, the development and understanding of the materials science of conducting barrier layers is possibly the most important. We address this topic next.

3.2.1. Conducting barrier layers for high-density architectures

A key aspect of cell architecture for a high-density memory technology shown in Fig. 24 is that bottom electrode of the ferroelectric capacitor is in direct electrical contact with the drain of the pass-gate transistor. This immediately puts drastic materials constraints, since oxidation of the poly-Si plug has to be avoided at all costs. Furthermore, Si out-diffusion and lead (or other cationic species) in-diffusion also have to be avoided. Therefore, suitable conducting barrier layers have to be used to prevent any undesirable interface chemistry. Clearly, Pt could be one such material; however, it forms a silicide in contact with Si, which is schottky in nature. Therefore, designing conducting barrier layers is an important task that is currently receiving the attention of process engineers and materials scientists in many laboratories. It should be noted that the conducting barrier layer technology is of critical value not only in the FRAM technology, but equally valuable in the DRAM technology.
TiN (which is a metallic compound) [94] and other crystalline and amorphous derivatives, in conjunction with Pt or Ir as a multilayered composite, have emerged as possible conducting barriers. We are studying the materials interactions, interface chemistry and structural integrity of (Ti, Al)N/Pt, Ir multilayers as a function of processing conditions. To understand the role of grain boundaries and grain size on the oxidation resistance and ferroelectric properties, we are using both single crystal Si[0 0 1] and poly-Si/Si substrates to grow the heterostructures. Some general comments regarding the structural integrity are in order. This is directly related to the oxidation of the TiN layer to TiO₂ and the volume change accompanying it (of the order of 60%). Oxidation of TiN is therefore accompanied by the peeling-off of the layers above the TiN layer and is visible even by optical microscopy. This occurrence is directly related to the crystalline quality of the Pt (or Ir) layer and its thickness. If this can be avoided, then one has to address second level problems, namely, the possibility of small amounts of oxygen that has diffused through the Pt (or Ir) layer and dissolved in the TiN layer, which leads to an increase in the resistance of this layer. Another important aspect is the possibility of internal stresses developing due to thermal expansion mismatch between the substrate and the various layers. Depending upon the nature of the stress (i.e. tensile or compressive), this can eventually lead to significant changes in the ferroelectric properties. It is thus clear that a complete understanding of the issues involved in the integration of ferroelectric capacitors on a poly-Si plug requires extensive investigations. We have begun this process by first studying epitaxial films, grown on a single crystal Si[0 0 1] substrate [95].

Detailed structural and microstructural investigations have been carried out on such epitaxial heterostructures. Under optimal conditions, we do not observe any lift-off of the layers, thus indicating that the TiN layer is still free of macroscopic oxidation. Transmission electron microscopy (TEM) studies of cross-sections confirm this, while the corresponding electron diffraction patterns reveal the cubic symmetry lattice parameters commensurate with that of the TiN layer [95]. An important point to note is that XRD studies show no evidence for a pyrochlore phase in the PZT layer. This is one of the most important benefits of using the conducting perovskite layer in the ferroelectric stack. As is always the case, the PZT and PLZT films with LSCO electrodes do not exhibit any fatigue, thus, further confirming that fatigue-free PZT-based films can be deposited on a viable conducting barrier layer structure. This approach still requires the use of protective Pt or Ir layers. Obvious concerns with the use of Pt or Ir are cost, availability and the lack of a suitable etching process. In view of this we have been investigating material systems that would eliminate the use of these noble metals.

Thin films of structurally amorphous metallic alloys, such as Cu–Zr, Ti–Si–N have been widely used as diffusion barriers in semiconductor metallizations, ultrahard coatings and as micromachining elements [96,97]. These applications take advantage of one or more unique properties of these films such as inertness to corrosive environments, electrical conduction or insulation, and the ability to remain X-ray amorphous up to processing temperatures. The reason for formation of amorphous phases of binary metallic alloys is been shown to be due to large differences in the atomic radii of the components, deep eutectics in the phase diagram and a strong affinity between the components of the alloy [98,99]. In addition, the presence of a predominantly covalently bonded species such as Al favors the formation of these phases. Controlling extrinsic parameters such as introducing O or N impurities and extremely high cooling or deposition rate have also been demonstrated to favor the formation of amorphous phases [100–102].

We are exploring the implementation of intermetallic alloys, both in crystalline and amorphous form, as barrier layers for high-density NVFRAM. Fig. 25 shows the hysteresis loops for a typical LSCO/PNZN/LSMO capacitor fabricated on poly-Si/Si using amorphous Ti–Al (a–Ti–Al) as a conducting diffusion barrier. The capacitors have a remnant polarization of ~28 μC cm⁻² and
coercive voltage of \(\sim 1\) V measured at 5 V in the geometry shown in the inset of Fig. 25 (i.e. vertical transport). They start to saturate at 7 V and have a resistivity of \(\sim 8 \times 10^9\) \(\mu\Omega\) cm (see Fig. 26). Further, although not shown here, the capacitors exhibited excellent fatigue and logic state retention properties [103]. These data indicate that no insulating layer is formed at the poly-Si/a–Ti–Al and a–Ti–Al/LSCO interfaces. For the case of the crystalline Ti–Al (c–Ti–Al) conducting diffusion barrier, the capacitors did not exhibit ferroelectric behavior. Capacitive coupling also yielded similar results suggesting a reaction between the bottom LSCO electrode and the c–Ti–Al layer.

Transmission electron microscopy studies were performed to investigate the interfaces in the two structures described above. Fig. 27(a) is a cross-sectional TEM image of PNZT/LSCO/a–Ti–Al/poly-Si/Si heterostructure. Notice the amorphous or nanocrystalline structure of the a–Ti–Al layer. As reported previously [103], there is no reaction at the LSCO/a–Ti–Al interface. Further, electron diffraction on the a–Ti–Al layer revealed that it is indeed amorphous. By contrast, the Ti–Al layer in Fig. 27(b) is clearly polycrystalline. The LSCO/Ti–Al interface (indicated by arrows) in Fig. 27(a) is abrupt, while there is a reaction zone at this interface for the sample cross-section shown in

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**Fig. 25.** Polarization hysteresis loops for a typical LSCO/PNZT/LSCO capacitor fabricated on poly-Si/Si using amorphous Ti–Al (a–Ti–Al) as a conducting diffusion barrier.

**Fig. 26.** Remnant polarization and coercive voltage for a typical LSCO/PNZT/LSCO capacitor grown on Ti–Al/poly-Si/Si. Inset shows the resistivity of the capacitors.
Fig. 27. Cross-sectional TEM image of (a) the α–Ti–Al/LSCO interface showing no reaction at the interface and (b) the c–Ti–Al/LSCO interface showing significant reaction as indicated by the arrows.

Fig. 27(b). The difference in the microstructure of the two Ti–Al layers appears to be the only property correlated to the observed difference in oxidation/reaction properties. This observation is consistent with the electrical measurements and also the milky color of the LSCO film deposited on the c–Ti–Al surface as opposed to the shiny black color of the LSCO film on the a–Ti–Al surface after deposition and annealing. The current (I)–voltage (V) characteristics of the LSCO/Ti–Al bi-layer was characterized using standard four-probe measurements in both the vertical and in-plane geometries to characterize the resistivity of the LSCO layer, as well as that of the Ti–Al/LSCO interface for both the amorphous and crystalline Ti–Al barrier layers. Fig. 28 shows the current–voltage characteristics of the Ti–Al/LSCO interface in the −5 to +5 V range. The a–Ti–Al/LSCO interface showed ohmic behavior (Fig. 28(a)) in the measured range with a resistance of ~30 Ω. In contrast, the c–Ti–Al/LSCO interface (Fig. 28(b)) shows a very asymmetric current–voltage behavior similar to that of a diode. For negative bias, there is a very small current that does not change with increasing voltage, while for positive bias, the current rapidly increases with increasing applied voltage. These data suggest that an interface layer is formed at the c–Ti–Al/LSCO interface, which may contribute to the diode-type behavior. This is consistent with the results of the TEM studies. Although further work is necessary to quantify the metallic (ohmic) character of the LSCO/a–Ti–Al interface, these results also qualitatively agree with the TEM analyses.
As mentioned earlier, although not shown here, these capacitors exhibited excellent fatigue and logic state retention properties [103]. We present only the results of dynamic imprint tests in Fig. 29. The primary experiment consists of a combined thermal and electrical (i.e. single-sided fatigue) stress profile that is impressed upon the test capacitor. To quantify the effects of test variables on imprint, we use the FOM (defined earlier). In this framework, FOM of ±1 would mean an imprint failure. As is clear from the figure, there is no imprint failure up to $10^9$ single side 5 V pulses at 180°C. As mentioned earlier, such a combined thermal and electrical stress profile is quite stringent and provides a rigorous measure of the quality of the ferroelectric capacitor.

4. Critical basic physics problems of NVFRAM: current understanding and opportunities

Several critical basic physics problems related to degradation processes need to be addressed and solved in order to develop reliable commercial NVFRAM. Several of these degradation
phenomena are due to complex defect chemistry and microstructure in the perovskite ferroelectric layer and/or the ferroelectric/electrode interface. Phenomena, which need to be understood and controlled, are discussed below.

1. Polarization fatigue (decrease in switched charge with the number of polarization switching cycles) is currently attributed to the pinning of domain walls due to electron injected through the electrode/ferroelectric interface into the ferroelectric layer and trapped in defects (most likely positively charged oxygen vacancies) [104]. Both oxygen vacancies in the bulk of the ferroelectric layer and at the electrode/ferroelectric interface appear to be contributors to fatigue.

2. Imprint is the tendency of a ferroelectric layer to switch its polarization direction to a preferential state after being polarized in that state many times and then polarized in the opposite direction (this phenomenon is also attributed to the trapping of electrons at defects in the ferroelectric layer).

3. Polarization retention relates to the capacity of a ferroelectric layer to maintain a certain level of polarization for long periods of time.

4. Leakage current is the phenomenon, whereby charges are lost from the capacitor; therefore, leakage should be minimized.

Materials integration strategies developed during the past 7 years resulted in the control of the capacitor degradation processes (fatigue, imprint and leakage) described above. In the case of PZT film-based capacitors, the main strategy involves using conductive oxide electrodes or hybrid oxide-Pt electrodes [105], where the oxide electrode layer is in contact with the PZT film to control oxygen vacancies and/or charge injection at the ferroelectric/electrode interface. In the case of the layered perovskite SBT, the degradation processes described above are controlled by the particular microstructure of the SBT material [106], where the oxygen vacancies and/or charge injection at the ferroelectric layer/electrode (mainly Pt) interface appears to be controlled by an oxygen-rich/Bi layer. On the other hand, there is comparatively less understanding of the basic mechanism for polarization retention (or equivalently retention loss) in ferroelectric capacitors. Recent work involving nanoscale imaging of ferroelectric domains [107], using a piezo-response atomic force microscopy technique, produced initial results, which suggest that retention loss occurs by a random walk-type depolarization process. The exact physical basis for the retention loss is still undetermined. Obviously, further work is necessary to unravel the details of the degradation mechanisms discussed above, since they have important implications for ferroelectric memory technology.

4.1. Finite size effects

Mitsubishi and Symetrix have fabricated patterned 1.0 μm capacitor arrays [108]. The actual ferroelectric capacitor dimensions for a 1 Gbit NVFRAM must have submicron lateral area and probably contain a ferroelectric layer about 50 nm thick. The effects of constrained geometries on ferroelectric capacitors are still largely unknown. Using a combination of focused ion beam milling and electric force microscopy (EFM), Ganpule et al. [109,110] have demonstrated that both PZT and SBT thin film capacitors can be scaled to at least 70 nm × 70 nm in lateral dimensions, as illustrated in Fig. 30. We expect future studies to evolve into further smaller sizes leading to the direct exploration of fundamental size effects and possible phase transitions driven by size constraints. Theoretical work (see [19] and references therein) indicated that depolarization fields in a typical ferroelectric capacitor with semiconducting electrodes would destroy the polarization switching
properties of ferroelectric layers thinner than 400 nm, while similar depolarizing fields would destroy the switching properties of ferroelectric layers only 4 nm thick when integrated with metallic electrode layers. Subsequent theories indicated that the minimum ferroelectric film thickness, which could sustain polarization switching, was about 2.5 nm [111]. However, recent experiments [112] have produced a critical ferroelectric layer thickness <0.9 nm. Scaling of ferroelectric and dielectric properties with both thickness and lateral dimensions needs to be understood through a combination of experimental (fabrication, testing) and modeling studies. The use of sophisticated tools such as focused ion beam milling, templated and/or self-assembled growth, scanning force microscopy and spectroscopy will be a strong focus of work in this area.

4.2. Stresses, clamping and the role of substrate-film interactions

The growth of ferroelectric thin films on substrates (which in most cases is Si) immediately places constraints, especially mechanically, which subsequently couples to the electrical and ferroelectric properties of the thin films. The magnitude of these coupling would likely depend on the coefficients in the Devonshire approximation of the free energy of the system. However, it is quite clear that the interplay between the mechanical properties of the substrate and the film can lead to suppressed polarization, dramatically decreased dielectric and piezoelectric coefficients, shifts in the phase transition temperatures and possibly impact the polarization dynamics (switching and
polarization relaxation). A simple illustration of the dramatic influence of the substrate (such as silicon) in producing a clamping effect on the piezoelectric response of the film is illustrated in Fig. 31. In this experiment, the ferroelectric PZT film has been fabricated into two types of test capacitors using focused ion beam milling [113]. The first type, which we call the ‘continuous’ consists of a continuous ferroelectric layer with only the top electrode fabricated delineated into the desired capacitor size. In the second type of capacitor structure (called ‘discrete’), the top electrode and the ferroelectric layer both are milled down to the desired size. Therefore, in this case, the lateral constraints in the ferroelectric layer are quite different than that in the continuous structure. Piezoelectric measurements using the AFM approach reveal dramatic differences in the piezo-response of the two types of capacitors; the ‘discrete’ capacitors show a piezoelectric coefficient ($d_{33}$), that is almost twice that of the continuous capacitor structure. The interplay between substrate and film mechanical properties and its impact on electrical properties should therefore be an important area of R&D in microelectronics. A similar approach is undoubtedly required in the broad area of ferroelectric thin films and we envision a strong focus on this topic in the future, especially as devices make their way into the market and long term reliability issues begin to dominate.

4.3. Polarization dynamics

We mentioned the role of stress in impacting the polarization dynamics in thin films. The area of polarization dynamics itself is critical not only from the basic science, but also from the device
Fig. 32. A schematic showing the interplay between processing microstructure and polarization dynamics over a broad time scale from 1 ps to 10 years. The regimes of interest in various phenomena are also indicated.

point of view. Indeed, it would be safe to assume that this is the most important of the fundamental topics that need a comprehensive and rigorous understanding, since this will ultimately impact the performance of ferroelectric devices. Polarization dynamics in ferroelectrics and dynamics encompasses a very broad bandwidth of time scales, from a few picoseconds for dipolar fluctuations in dielectrics, such as BST to the 10 year retention time for ferroelectric memories that is impacted by the time-dependent changes in the remnant polarization. This is schematically illustrated in Fig. 32. In between these two extremes, polarization switching occurs on time scale of a few nanoseconds, while relaxation phenomena in relaxor ferroelectrics occur over time scales of a few seconds and longer. The interplay between thin film processing, microstructure, domain structure and polarization dynamics is still poorly understood and will require measurements of carefully prepared and characterized test structures. We envision the dominant role of novel probes to understand the physics of polarization dynamics, with different probes impacting the various time scales involved. In Fig. 33, we illustrate the use of three such novel probes to study dynamics in three time scales. We envision probes such as the scanning microwave microscope and optical probes such as femtosecond optical spectroscopy to be of great value in understanding temporal fluctuations and spatial variations of the dielectric responses (dielectric constant, loss tangent, polarization, etc.), especially at very short times. We also expect optical probes to be a key component in understanding the switching dynamics with high temporal resolution in ferroelectric films. Finally, we expect techniques such as the EFM to be of immense value in understanding polarization relaxation phenomena with high spatial resolution. Indeed, this is already well underway, and we present one example of the use of EFM techniques to image polarization relaxation effects. We note that one common theme in all of these novel probes is the pervasiveness of scanning processes to obtain spatial images of physical properties.

We illustrate the impact of EFM techniques through a study of retention loss in thin film ferroelectrics [114]. Fig. 34 illustrates schematically the general approach behind the use of a standard AFM to carry out piezoelectric imaging, the details of which are reviewed elsewhere. In short, a low frequency ac signal imposed on the metallized AFM tip generates a piezoelectric response from the ferroelectric, which results in a height change of the surface. This is dependent
on the sign of the polarization (i.e. $\pm P$) and can then be imaged as regions of bright or dark contrast, which represent positive and negative polarization states. Fig. 35 illustrates how this approach can be used to image polarization relaxation. Fig. 35(a) is the EFM image of an epitaxial film with an epitaxial LSCO bottom electrode. The asymmetric electrode configuration leads to a preferred polarization state, which is imaged with bright contrast in the outer portion of this figure (depicted as the as-grown stable state). The orthogonal lenticular features are arrays of 90° domains that form to relieve the elastic strain. Using a dc bias superimposed on the AFM tip, the central portion of this image was switched from the stable state to the unstable state (in dark contrast). One can then use the EFM to probe the relaxation dynamics of the unstable state to the stable state as shown in Fig. 35(b–f). Detailed analysis of the fraction reversed as a function of time reveals a stretched exponential type relaxation [114], the fundamental origin of which is still unclear. Therefore, fundamental studies, including direct observations of the relaxation processes, correlation to macroscopic measurements on discrete capacitors and integrated memory cells, and the development of mathematical models to understand and predict the relaxation behavior are required. The role of fluctuations (thermal, electrical, chemical, dipolar, etc.) and perturbations (structural, chemical electrical, etc.) on the polarization dynamics should prove to be a fertile area of fundamental research in the future. We note that there has been a considerable body of work on two other aspects of polarization dynamics in polar ferroelectrics, namely, fatigue and imprint. Although these two problems were identified in the early years as ‘show-stoppers’, it is safe to say that although there are technologically viable solutions to both these problems, the fundamental understanding is far from complete.
4.4. Role of defects

The impact of defects is one area that is possibly strongly overlooked. Although considerable amount of defect chemistry understanding is already in place for bulk ferroelectrics and dielectrics (e.g. PZT, BST), there is very little work on the characterization (by direct means) of defects in thin films. This is especially true of point defects such as oxygen vacancies and cationic defects, both of which are considered as critical in determining the properties of ferroelectrics and dielectrics. Direct determination with high spatial resolution and compositional precision of the defect chemistry in thin films still remains an unresolved paradigm. We believe that this complex problem will have to be addressed at some point in the evolution of integrated ferroelectric devices. The interested reader is referred to reviews on the defect chemistry of functional perovskite-type oxides, such as PZT, BST and SBT [115,116].

5. Future technology directions

The next generation of high density NVFRAM will have nearly identical cell structures as the stacked cell DRAMs using high-dielectric constant materials such as BST (BaTiO$_3$), PZT and Ta$_2$O$_5$. This means that NVFRAM can now enjoy all the process tools developed for DRAMs, and go one step further in functionality by providing non-volatility at low power. In the stacked-cell
configuration, a high-quality ferroelectric thin film needs to be deposited with good step coverage, which can be obtained by MOCVD [117] or LSMCD [118]. Further discussion on integration issues will be given, which will show that stacked-cell processing of NVFRAM significantly simplifies the add-on ferroelectric capacitor module. Advanced MOSFETs for logic and other general uses are also adding Ta2O5 layers in the gate stack. This is required because the demands of CMOS for thinner gate dielectrics have been found to be very difficult to satisfy by simply reducing the SiO2 thickness. Furthermore, the FLASH memory cell is being transformed by adding a ferroelectric switching gate in place of programming by tunneling. This evolution changes the scaling rules for FLASH radically and allows significant improvements such as writing speed, which could be equal to that of DRAMs. As mentioned above, use of ferroelectric perovskites with film thickness 100 nm yields NVFRAM write voltage of about 1 V. Writing speeds ≤6 ns can be achieved at the capacitor level, even for capacitors with thick ferroelectric films (≥180 nm) and large areas. For these devices, the speed is limited by the CMOS, not by the intrinsic characteristics of the ferroelectric layer, non-volatile ferroelectric random access memories (NVRAM) are the only fast write non-volatile memories existing today. This characteristic and the nearly fatigue free behavior with low power make NVFRAM the mature evolution of CMOS in the non-volatile memory area.

Currently, and in the foreseeable future, NVFRAM have the potential of impacting three major markets in the $150B dollar range. First, as stand-alone memories, NVFRAM will be in direct
competition with FLASH, EEPROMs, DRAMs and SRAMs based on cost and density. However, in many cases, density and even cost may not be as important as high-speed write and non-volatility. In the second market, NVRAM are already enjoying a great position in cost and functionality. In this case, the fast write speed and low power allows the use of smart cards or tags in a variety of applications such as ticketing, fare collections and inventory control. Finally, where the logic unit is a microcontroller or digital signal processor (DSP), NVFRAM already has shown interesting ‘system-on-chip’ capabilities without the added complications of power transistors such as in EEPROMs and FLASH. Also, smart cards with embedded microcontroller have demonstrated that NVFRAM are poised to enter this market.

In summary, NVFRAM are entering commercialization as stand-alone memories (in low and medium densities), contactless cards and tags, and in embedded microcontrollers. These are also among the fastest growing segments of the semiconductor industry. Adding to this, the prospect of BST in DRAMs, ferroelectrics have entered the semiconductor device world in almost every market segment.

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