Chemical vapor deposition of rough-morphology silicon films over a broad temperature range

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Growth of rough polycrystalline silicon films has been achieved on SiO2 surfaces over a broad temperature range (>100 °C) using SiH4 chemical vapor deposition at low pressures (mTorr range), with smaller grain structure and roughness length scale achieved at lower temperatures. Rough morphology over a broad temperature range is attributed to the combination of nucleation-controlled initial growth (on SiO2) and domination of growth by surface reaction (cf. gas phase).

Increasingly high density storage capacitor structures are needed for high density dynamic random access memory (DRAM) memory cells, decoupling capacitors in bipolar technology, and storage capacitors for thin film transistors used for driving liquid crystal displays. As the DRAM memory cell size decreases, “texturing” (or roughening) of the capacitor's polysilicon (“poly-Si”) bottom electrode to increase its effective surface area has attracted significant interest as an alternative to yet thinner oxide/nitride insulator films or development of high dielectric constant insulators [e.g., TiO2 (Refs. 10 and 11) or PZT (Refs. 12 and 13)]. Such rough surfaces might be useful in other applications as well, such as in the fabrication of low-stiction thin magnetic disks.

The first approaches to fabricate rough polysilicon films employed (i) reactive ion etching or (ii) thermal oxidation of poly-Si followed by selective etching of the oxide along doped grain boundaries; however, relatively high temperatures are required for poly-Si growth and thermal oxidation.

More recently, direct growth of rough Si films has been demonstrated. In one approach, amorphous Si films without native oxide were annealed in high vacuum to achieve capacitor area enhancement of 1.8; this is believed a consequence of the high mobility of Si atoms on the clean Si surface, leading to hemispherical grain surface structure. In a related approach, conventional low pressure chemical vapor deposition (LPCVD) SiH4 processes at 1 Torr have yielded effective area enhancements of ~2.1–2.5×, as determined from measurements of capacitors formed on the rough Si surfaces. In these experiments, substantial Si surface roughness and capacitance enhancement was obtained only in a narrow (≤10 °C) window of deposition temperatures centered at ~550 °C. Since this is the boundary between amorphous and polycrystalline Si growth, the roughness mechanism appears associated with a delicate balance of kinetics between surface deposition/growth and surface diffusion. Although conventional LPCVD reactors are nominally capable of temperature uniformity and reproducibility of order 1 °C or better, manufacturability at VLSI/UlSI integration levels would be a severe concern with a temperature window of only ~10 °C as full width at half-maximum.

We report here the first demonstration of direct CVD growth of rough Si films over a much broader temperature range (>100 °C) than previously obtained, carried out by SiH4 growth (undiluted) on SiO2 surfaces at relatively low temperatures (<600 °C) and at low pressures (a few mTorr). Under these conditions we believe that the broad temperature window for rough Si film morphology is achieved through the combination of nucleation-controlled initial growth (on SiO2) and domination of growth by surface reaction (cf. gas phase).

Experimental techniques have been described previously. Briefly, the substrates were (100) Si wafers with a thermal oxide ~22 nm thick, RCA cleaned and ultraviolet (UV) ozone treated before insertion into the reactor, a quartz-wall, lamp-heated, single-wafer ultrahigh-vacuum-based CVD system. Thermally programmed hydrogen desorption measurements were alternated with growth cycles in order to titrate the total amount of deposited, exposed Si surface area on the wafer, from the submonolayer regime to the formation of thin Si films (100 nm thickness range).

The elemental Si surface area, obtained from integrated hydrogen desorption flux, is shown in Fig. 1 as a function of total growth time for SiH4 growth at 1.6 mTorr pressure and 550 °C wafer temperature. The nonlinear initial behavior suggests (14,15) nucleation-controlled initial growth of Si on the SiO2 surface. Most important for this study is that the exposed surface area rises well above the value for the flat Si(100) surface, by >35%, reflecting enhanced surface area as microscopic roughness of the deposited Si film as compared to the area for a flat oxide-free Si(100) wafer. Upon further growth, the exposed Si surface area decreases to the smooth-surface value, suggesting an eventual smoothing mechanism.

In the present experiments, desorption monitoring of surface area enhancement was used to determine in situ the SiH4 exposure time at which a maximum surface roughness occurred, following which growth was terminated and the wafer was removed to study surface morphology and microstructure. Typical scanning electron micrographs (SEMs) for Si films grown at 1.6 mTorr and temperatures...
510, 525, 540, and 570 °C are shown in Fig. 2, revealing clearly that significant surface roughness of the grown Si film is obtained over a wide range of growth temperatures. Indeed, we have observed analogous roughness behavior for growth temperatures from ~480 to ~600 °C, i.e., a process temperature range >100 °C. For a given growth temperature, the morphological features suggest a characteristic feature size determined by the largest nuclei (i.e., those nucleated at the earliest stages of film growth). Since the morphological characteristics (average feature size, density, and shape) change continuously with growth temperatures, there appears the possibility of morphology and roughness control as part of the process.

Atomic force micrographs of these samples were taken using a Nanoscope (Digital Instruments), some of which are shown in Fig. 3. The morphology appears rounded in shape for lower growth temperature (525 °C), but with higher growth temperature (570 °C) there is substantial evidence of faceting (as well as larger features), indicating formation of larger grain crystals as expected for poly-Si grain growth. Since roughness is achieved whether or not faceting occurs, it appears that the mechanism exploited here to achieve rough surface morphology over a broad temperature range is rather independent of the growth mode (i.e., amorphous versus polycrystalline).

The surface area enhancement of ~1.35× inferred from desorption measurements and seen in Fig. 1 is consistent with the roughness characteristics shown in Figs. 2 and 3. From simple models of contacting hemispheres on a flat surface, we estimate a roughness-related area enhancement of \( \frac{\pi}{2} = 1.57 \times \) for a cubic and \( \pi/\sqrt{3} = 1.81 \times \) for a hexagonal arrangement of hemispheres. If one further takes into account a filling coefficient due to smaller nuclei between the initial nuclei, as has been observed in SEM micrographs,\(^{15}\) the enhancement over a flat surface be-
comes $\pi/2(1 + 1 - \pi/2) \sim 2$. We believe that the somewhat lower value of the surface area enhancement ($1.35 \times$) suggested by the peak in Fig. 1 is a consequence of temperature nonuniformities across the wafer, which have been observed by pyrometry and film thickness measurements; such nonuniformities would lead to a distribution of surface area versus growth time curves like that in Fig. 1, thereby broadening the net curve and suppressing the height of the peak. Thus, the $1.35 \times$ enhancement factor represents a lower bound for roughness enhancement of surface area.

Growth kinetics in the few mTorr regime are nucleation-controlled and dominated by heterogeneous (surface) reaction. In the present case of Si growth on SiO$_2$, a low density ($\sim 10^{15}$/cm$^2$) of initial Si nuclei are essentially formed randomly on the surface. As shown by cross-sectional SEM this random pattern provides a roughness template: selective surface reaction leads to deposition primarily on existing nuclei, i.e., causing additive pattern transfer to finally form a roughness pattern on the Si film surface which replicates the roughness template of initial nuclei.

The roughness behavior and mechanisms reported here are clearly different from the amorphous-to-crystalline transition invoked in previous work to explain the very narrow temperature window for rough Si growth observed under conventional LPCVD conditions (>100 mTorr). These higher pressure conditions also present the possibility of gas phase nucleation and reaction, yielding more reactive gaseous intermediates for enhanced Si nucleation rate on the SiO$_2$ surface, or small particles for deposition on the surface; either case could prevent nucleation and selective surface reaction from determining the resulting film's surface morphology.

We have also grown rough Si films over a broad temperature range under batch, hot-wall reactor conditions like those employed in UHV/CVD. The key element is to maintain reaction pressures sufficiently low that nucleation on SiO$_2$ and selective growth on existing Si nuclei dominate deposition.

In summary, we have achieved the growth of rough Si films over a wide temperature range (>100°C) and with control over roughness length scales. This process temperature latitude is necessary (though not necessarily sufficient) for exploiting rough Si electrodes to enhance capacitance density for advanced DRAM manufacturing.

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