and is expected to be important in submicron CMOS.

In submicron CMOS, the well dopant concentration is expected to increase to avoid punchthrough and other short-channel effects. With an increase in the well concentration comes an increase in junction capacitance. With the problems of hot electron effects affecting gate oxide reliability, it is unlikely that gate-oxide thickness will be scaled as aggressively as the past. This results in gate oxide capacitance remaining stable. Hence, scaling to submicron will result in the junction capacitance becoming a larger portion of the total capacitance in a circuit. In CMOS/SOI, the junction capacitance is fixed as the dielectric layer thickness remains the same with scaling. Hence, it is expected that the total capacitance in an SOI structure will become increasing smaller compared to a similar bulk structure. If CMOS/SOI devices have the same driving capability of comparable bulk CMOS devices, the lower total capacitance will result in a faster overall circuit.

Spurious charges are generated in a circuit by cosmic rays or by alpha particles, which are generated when radioactive trace elements in packaging materials decay. These energetic particles generate electron-hole pairs in the silicon wafer. If these charges are collected at critical nodes of the circuit, circuit upset or electronic memory upset, commonly known as soft error, occurs. As device feature sizes become smaller, the critical charge required to upset them becomes smaller. Hence, it is expected that electronic circuits will be more susceptible with scaling. In SOI structures, the active devices are separated from the bulk wafer by the dielectric layer, and charges generated in the bulk wafer will not be collected in the active devices. Hence, SOI devices are known to be more resistant to upsets and soft errors. Partly for this reason, SOS circuits have been chosen for use in space-borne electronics and avionics.

Interest in SOI also comes from users of bipolar circuits for many of the same reasons stated above. In addition, it will be easier to implement complementary bipolar circuits with SOI. SOI also makes possible the horizontal bipolar structure, which can significantly improve the packing density of bipolar circuits to match that of MOS.

Dielectric isolation and junction isolation techniques have been used extensively for high voltage device and high voltage integrated circuit applications. However, these techniques are, in most cases, not compatible with VLSI techniques. The trend of high voltage integrated circuits is to include more and more low voltage control functions on the same chip as the high voltage power devices. This integration can easily be implemented on SOI technologies, and it is expected that SOI will be used in an increasingly larger number for these applications.

Several new SOI technologies including implanted buried oxide layer, full isolation by oxidation of anodized silicon, epitaxial overgrowth, and beam recrystallization have been studied to achieve SOI structures. The advances made in these technologies to date will be discussed.

* Present address: LAM Associates, P.O. Box 742943, Dallas, Texas 75374.

Summary Abstract: High temperature decomposition of SiO₂ at the Si/SiO₂ interface

IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598

(Received 7 November 1985; accepted 16 December 1985)

In spite of the extensive investigations of Si oxidation reactions which have been carried out in past years, the process of oxide decomposition has received little attention, even though it is known to occur in the temperature range of thermal oxidation or slightly above. The decomposition and removal of SiO₂ are known to provide atomically clean Si surfaces, a procedure already exploited in fundamental surface science studies. High temperature processes (in addition to thermal oxidation) have profound technological consequences: postoxidation inert gas annealing at temperatures approaching oxide decomposition temperatures is required to achieve the extremely high quality Si/SiO₂ interface properties which form the basis for current Si FET integrated circuit technology.

In an effort to understand the microscopic chemistry of the oxide decomposition process, we have studied the consequences of high temperature annealing of thin (50–500 Å) thermal oxide films carried out in ultrahigh vacuum conditions to assure that negligible oxygen is present for reoxidation of the surface. In contrast to the high uniformity of the oxidation reaction, the decomposition of the oxide proceeds in a very nonuniform way: holes form in the oxide and grow until the oxide is completely removed from the surface, but in intermediate stages the remaining oxide on the Si surface retains its original thickness until removed by lateral growth of the holes.

High resolution medium energy ion scattering measurements, carried out at the F.O.M. Institute in Amsterdam, reveal the depth profile of Si and oxygen composition with a very high depth resolution of the order of 3–5 Å. Upon annealing at 1100°C, the ion scattering spectra for 120 keV He⁺ ions evolve continuously from that of a complete oxide layer on Si to that of a clean Si surface. At intermediate stages, however, the spectra appear as a superposition of complete oxide and clean Si spectra. The oxide thickness remains unchanged; only the intensity of the oxide spectrum
is reduced as the intensity of the clean Si spectrum increases. This demonstrates clearly that with annealing the portion of the surface covered by oxide decreases, while progressively more of the surface area is comprised of atomically clean Si.

The shape of the growing regions of clean Si surface resulting from ultrahigh vacuum annealing is revealed in optical, scanning electron, and Auger micrographs. The oxide is absent from nearly circular regions, or holes, of several microns diameter typically, once a notable fraction of the oxide is removed. These hole regions are sufficiently free of oxide so that the exposed Si surface in the holes yields a (2×1) LEED diffraction pattern even when half the surface area or more remains oxide-covered. These holes apparently nucleate around defects in the oxide or at the interface, then grow in diameter with annealing time. Scanning Auger micrographs distinguish clearly that the oxide is present between, not in, the circular hole regions.

Cross-sectional TEM observations show the vertical structure of the holes, particularly at their periphery. The oxide sidewall is undercut, suggesting that the decomposition reaction occurring at the periphery of the hole takes place primarily near the Si/SiO₂ interface. Furthermore, excess Si is seen against the oxide sidewall, while some notable amount of Si has been etched away from the bottom of the hole (i.e., out of the Si substrate); these observations suggest that the reactant Si atoms are provided by surface self-diffusion of Si across the bottom of the hole. This would provide a consistent microscopic picture for SiO₂ decomposition at the hole periphery, and hence hole growth, by the reaction

\[ \text{Si} + 3 \text{SiO}_2 \rightarrow 2 \text{SiO}_2^+. \]

The mechanisms responsible for hole initiation or nucleation remain unclear and an important subject for further study. The prominent lateral inhomogeneity of the reaction suggests that defects play an important role in the decomposition process. Because high temperature processes are used in oxidation and postoxidation steps in FET technology, the oxide decomposition process may have important practical implications.

Acknowledgments: We are grateful to P. S. Ho, F. W. Saris, J. F. van der Veen, and F. M. d'Heurle for useful discussions. This work is sponsored by F.O.M. with financial support from Z.W.O and by the Office of Naval Research. Two of us (G.W.R. and R. M.T.) thank Dr. J. Los and the F. O. M. Institute in Amsterdam for their hospitality.

*1 Permanent address: Institute of Semiconductor Electronics, Technical University, Aachen, Federal Republic of Germany.