Tungsten Nitride Barrier/Tungsten Via to Copper Interconnect for Memory Device Applications

Juwen Gao, Josh Collins, Wei Lei, Michal Danek, SungHyun Hong, Kaushik Chattopadhyay, Tom Mountsier, and Roey Shaviv
Novellus Systems Inc., San Jose, CA, 95134

ABSTRACT

In this paper, we report a novel, high productivity and low cost integration scheme for copper interconnects in memory devices using a tungsten nitride barrier and a tungsten via. Key integration challenges overcome in this work include zero sputter Cu_2O reduction, damage-free conformal WN barrier deposition, void-free W fill, and W CMP with minimal dishing, plug coring, or barrier erosion. Electrical results show high via chain yield with a tight distribution in via chain resistance. Electromigration results show comparable mean time to fail to that of the Cu-only control. Effects of WN film thickness, preheat time and WN deposition temperature were investigated.

INTRODUCTION

With increasing demand on speed and device density, copper interconnect has been introduced into Flash and DRAM devices. Tungsten still remains as the material of choice for the via as shown in figure 1. The tungsten via to the Cu interconnect brings new integration requirements and challenges to the conventional liner/barrier scheme. For example, in the conventional Ti/TiN liner/barrier approach, a bi-layer of PVD Ti/MOCVD (metal organic chemical vapor deposition) TiN is required [1]: PVD Ti is deposited at the contact bottom for copper barrier followed by a MOCVD TiN barrier layer to prevent Ti from fluorine attack during the subsequent CVD-W fill. This bi-layer scheme has several limitations: i) poor PVD-Ti step coverage, ii) PVD-Ti overhang, iii) MOCVD TiN film needs to be thick and dense enough to be an effective barrier, making this scheme more costly and less extendable. In addition, it was reported that SiH_4, which is typically used in CVD-W nucleation step, can easily diffuse through MOCVD-TiN [2, 3]. The penetration of SiH_4 to the underlying copper may lead to formation of high resistivity CuSix.

Pulse nucleation layer deposition (PNL) of WN/W vias can overcome these limitations. PNL is capable of depositing highly conformal WN/W films [4,5]. PNL-WN has good adhesion on dielectric and is an excellent barrier for copper and SiH_4 diffusion. Therefore, a single thin layer of PNL-WN can replace Ti/TiN as both the diffusion barrier and the liner.

In this paper, we report a W via integration scheme for copper interconnects, using PNL-WN as the barrier and PNL-W for via fill. Process characteristics are summarized and electrical performance of this process flow is also evaluated.

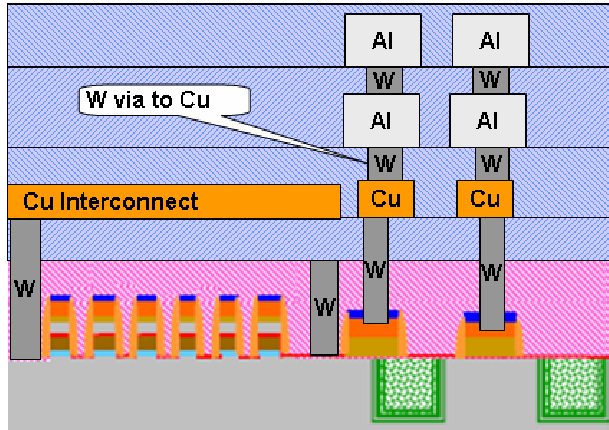


Figure 1. A typical NAND Flash structure with copper interconnect

EXPERIMENT

The PNL-WN/W via deposition was performed in a Novellus 300mm DirectFill™ system. The system consists of a preclean module, a PNL-WN deposition module and a PNL-W fill module. The multi-station sequential deposition (MSSD) architecture of PNL-WN module enables simultaneous processing of four wafers in each module, resulting in a high throughput. The MSSD architecture also allows individual control of gas flows, deposition temperatures, and step times at each station to optimize performance for each process step.

Ar/H_2 plasma was used to clean Cu_2O. The process pressure was 10mTorr to 100mTorr. The plasma power was 1000W to 3000W. The wafer bias power was 0 to 300W.

The PNL WN barrier deposition process is a thermal ALD process at temperatures between 200 to 400˚C and a pressure of 1-10 Torr. One deposition cycle consists of sequential exposure of B_2H_6, WF_6, and NH_3. Each precursor exposure was followed by an Ar purge (Figure 2). The cycle is repeated until desired film thickness is obtained.

Tungsten fill is accomplished by a PNL-W nucleation (sequential introduction of SiH_4 and WF_6 reactive gases at 300 ºC) followed by a conventional WF_6-H_2 CVD plug fill at 395 ºC, both at 40 Torr. Details of PNL-W fill process can be found in the literature [5].

Tungsten chemical-mechanical-polishing (CMP) was carried out on a Novellus Xceda™ tungsten CMP system.

Cu_2O thickness was measured using reflectivity. WN film sheet resistance and thickness were measured by four-point probe and x-ray fluorescence (XRF) respectively. WN barrier property to SiH_4 diffusion was evaluated by SIMS (secondary ion mass spectroscopy) depth profile analysis. Both top-view and cross-section scanning electron microscope (SEM) were used for post-CMP defect inspection. Novellus internal test structure wafers (with M1 and M2 Cu interconnects connecting through 90 nm via) were used in the integration test.

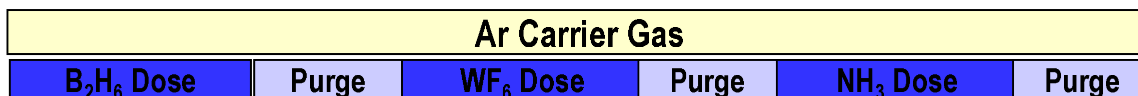


Figure 2. Schematic of PNL-WN deposition sequence

DISCUSSION

Via bottom Cu_2O clean

Cu at the via bottom can be easily oxidized in the atmosphere after via etch. Cu_2O will increase the electrical resistance of the via due to its highly insulating nature and therefore needs to be removed before barrier deposition. In this work, an Ar-H_2 plasma was used to reduce Cu_2O to copper. The plasma was carefully-controlled to avoid Cu sputter, which could degrade the reliability of the devices.

Cu_2O removal was characterized using a 120Å Cu_2O film grown by thermal oxidation of a 1000Å PVD-Cu film. This film was subjected to Ar-H_2 plasma to reduce Cu_2O at different clean times. Optical reflectivity at wavelength of 550nm was measured and converted to Cu_2O thickness on copper [7]. As shown in figure 3, an Ar-H_2 plasma can effectively remove Cu_2O. XRF measurement of the Cu substrate before and after preclean showed zero Cu sputter loss.

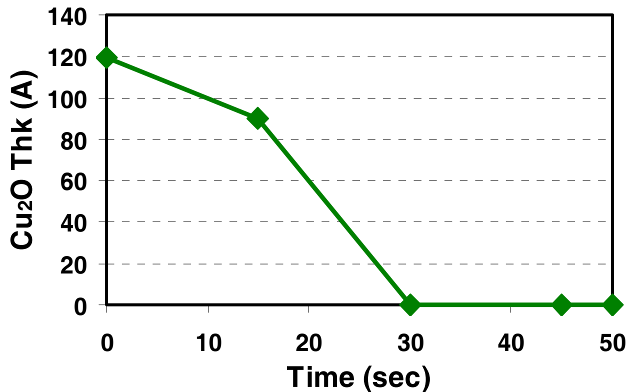


Figure 3. Cu_2O reduction by Ar-H_2 plasma

WN barrier/W process

The WN deposited by the PNL process has a growth rate of 2.1 Å/cycle. The ALD process nature produces a film of WN with excellent step coverage. XRD analysis shows that the WN barrier layer is polycrystalline β-W_2N, which provides a superior diffusion barrier property [5].

It should be pointed out that Cu itself is non-reactive with WF_6 and HF (positive Gibbs energy of reaction under typical deposition conditions) and thus requires no special protection. However, SiH_4 from the subsequent tungsten nucleation process may diffuse through the barrier into the copper layer and form highly resistive copper silicides. To evaluate the barrier performance of PNL-WN film for SiH_4 diffusion, 1000Å of PVD-Cu films with different thicknesses of PNL-WN were exposed to a PNL-W nucleation process which uses SiH_4-WF_6 at 300 ºC. SIMS analysis (Figure 4) shows that without WN film, there is a significant amount of silicon diffused into the copper film. As thin as 20Å of WN film effectively blocks diffusion of SiH_4 into Cu.

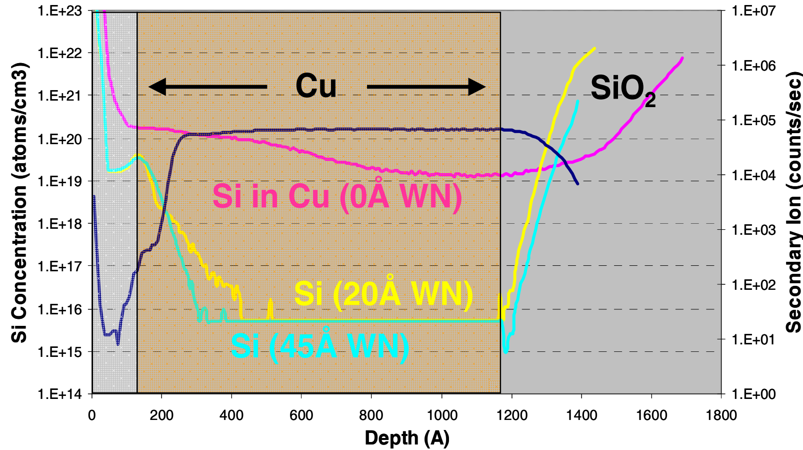


Figure 4. SIMS analysis showing Si in Cu with and without WN barrier.

After WN barrier deposition, the vias were filled with PNL-W. The PNL-W provides excellent via fill capability [6].

A TEM image of a single contact via showed a very clean copper-tungsten interface without any sign of fluorine attack or SiH_4 diffusion to the copper layer (Figure 5). Due to the conformality of WN there is no void at the Cu-WN or Cu-SiN interfaces.

Barrier adhesion to the dielectric and copper layer meets requirements as verified with scribe-tape test on blanket wafers with full WN/W (2000 Å) stacks.

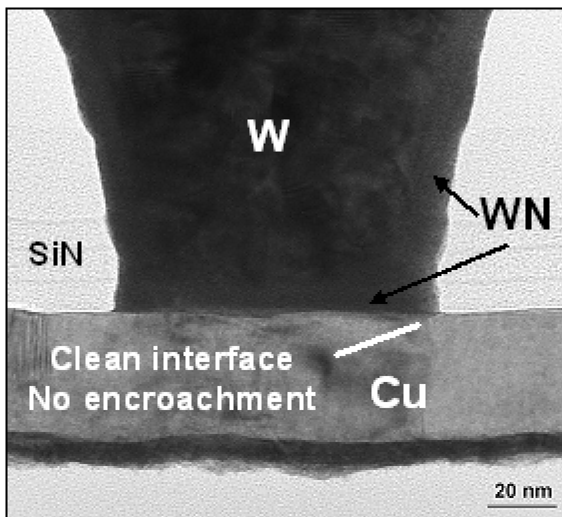


Figure 5. Cu/WN interface with PNL-WN/W fill

Tungsten CMP

Tungsten CMP is a key step in the integration. Top-view SEM inspection indicates that PNL-WN/W fill integrates well with CMP. No via coring or barrier erosion was observed. A cross-section SEM image after CMP (Figure 6) shows excellent CMP performance. Note that an oxide buffing step was applied after tungsten polishing to allow plug extrusion such that there was no post-CMP cleaning residue remaining at the top of the plug after CMP.

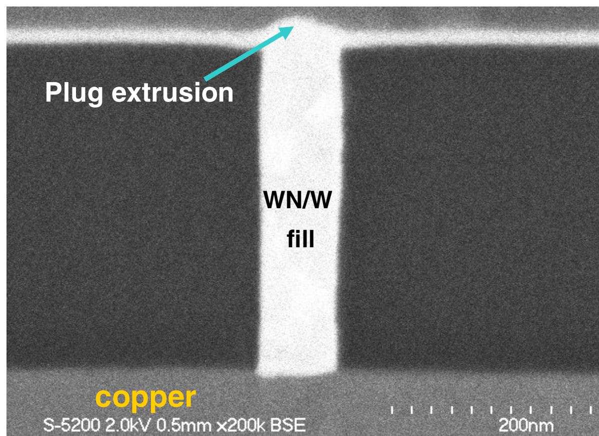


Figure 6. Cross-section SEM image of WN/W via to Cu after CMP and M1 deposition

Electrical performance

Electrical testing was carried out using Novellus internal test structures with 90nm tungsten vias between Cu metal-1 and metal-2 layers. Both Kelvin and chain contact resistances were measured. The effect of WN film thickness, preheat time and WN deposition temperature were explored.

As can be seen from figure 7a, there was no significant effect on Kelvin contact resistance related to preheat time and deposition temperature. As expected, a thinner (45 Å) WN layer results in lower via resistance. Figure 7b demonstrates the via chain parametric yield on 2 million vias for the baseline condition where 65 Å of PNL-WN was used as the barrier. Nearly 100% chain yield was achieved with very tight distribution.

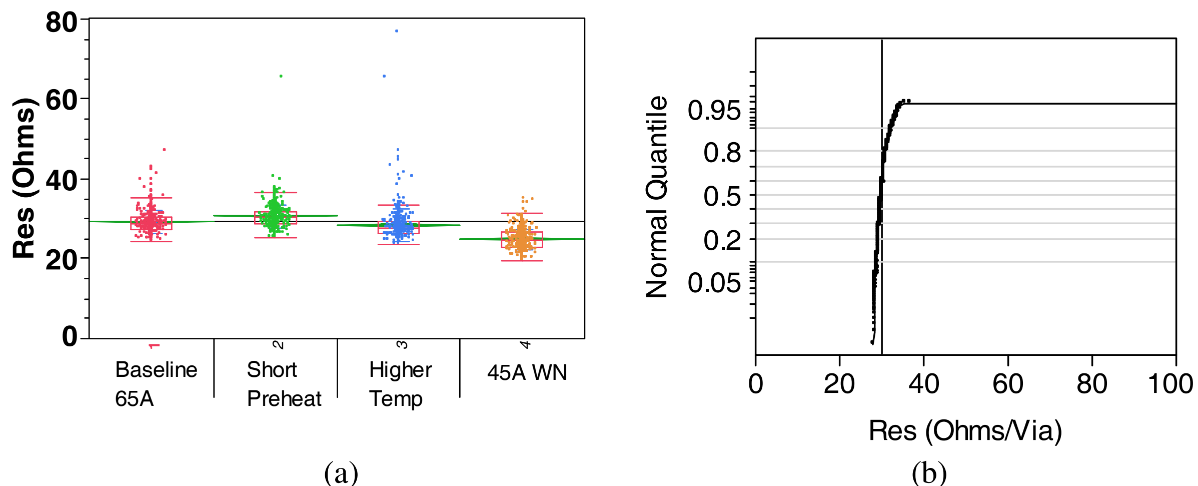
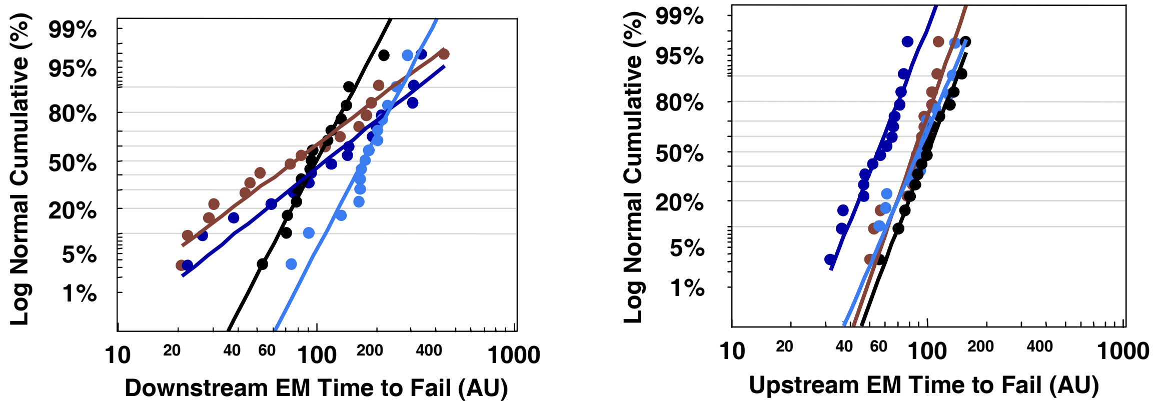


Figure 7. Parametric performance for 90nm vias : (a) Kelvin via resistance ; (b) Rc yield for 2 million via chain (baseline WN 65 Å)

Electro-migration performance

Downstream and upstream electromigration (EM) results are presented in figure 8. These were compared to a dual damascene all-copper control. Package level EM testing was conducted

at 325° C using a current density of 2.5 MA/cm^2. A wider distribution (σ ~ 0.8) in downstream EM time to fail is observed for the baseline process relative to control (σ ~ 0.3). Mean time to fail (t_{50}) for the baseline process is comparable to that of the control. Shorter preheat has no effect on downstream EM as both t_{50} and σ are similar to that of the baseline process. J_{max} with these WN conditions is about 3 MA/cm^2. Downstream EM of the higher temperature WN process has a t_{50} that is about 2 times longer than that of the control with a similar distribution (σ ~ 0.3). Consequently, with these conditions J_{max} is > 10 MA/cm^2 and is significantly larger than results for the control where J_{max} ~ 7 MA/cm^2. Short preheat appears to be detrimental to upstream EM where t_{50} is about half that of the control and J_{max} is about 7 MA/cm^2. The upstream EM results with all other processes are statistically equivalent to those of the copper control. For upstream EM, J_{max} > 10 MA/cm^2 for all these process conditions.



a. *b.*

Figure 8. Downstream (*a.*) and upstream (*b.*) EM time to fail for: Cu control (black), baseline WN/W (brown), short preheat (dark blue), and high temperature WN (light blue).

CONCLUSIONS

A PNL-WN/W via has been applied to Cu interconnect. The integration scheme includes plasma preclean, WN barrier deposition and W via fill. It was demonstrated that Ar/H_2 plasma clean can effectively remove Cu_2O. The highly conformal ultra thin PNL-WN film has excellent step coverage, superior barrier property to SiH_4 diffusion and good adhesion to both Cu and dielectrics. CMP integration was very successful with low defects counts. Parametric electrical tests showed that there was no significant impact of process temperature and preheat time. A thinner WN layer results in lower via resistance. Nearly 100% yield was achieved for 2 million via chains with 90nm via structure. Finally, electromigration performance was comparable to copper control. In summary, the low cost, high productivity PNL-W/WN via scheme in this work is a viable solution for the via to copper interconnect in memory applications.

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